Bosc 5.Y
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CHAPTER 20

Load Lines And DC Bias Circuits

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20.1. DC Load Line

For drawing the dc load line of a transistor, one need to know only its *cut-off* and *saturation points*. It is a *straight line* joining these two points. For the *CE* circuit of Fig. 19.17, the load line is drawn in Fig. 20.1. *A* is the cut-off point and *B* is the saturation point.

The voltage equation of the collector-emitter is

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L}$$

Consider the following two particular cases :

(*i*) when $I_C = 0,\ V_{CE} = V_{CC}$

— cut-off point *A*

(*ii*) when $V_{CE} = 0,\ I_C = V_{CC}/R_L$

— saturation point *B*

Obviously, load line can be drawn if only V_{CC} and R_L are known.

Incidentally slope of the load line $AB = -1/R_L$.

Note. The above given equation can be written as

$$I_C = -\frac{V_{CE}}{R_L} + \frac{V_{CC}}{R_L}$$

It is a linear equation similar to $y = -mx + c$.

The graph of this equation is a straight line whose slope is

$$m = -1/R_L$$

B° 259 × 39 × 20 =

Active Region

All operating points (like *C*, *D*, *E* etc., in Fig. 20.1) lying between cut-off and saturation points form the *active region* of the transistor. In this region, *E/B* junction is forward-biased and *C/B* junction is reverse-biased—conditions necessary for the proper operation of a transistor.

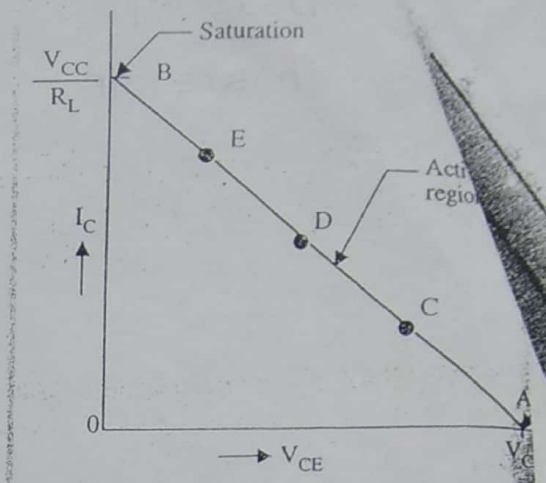


Fig. 20.1

Quiescent Point

It is a point on the dc load line, which represents the values of I_C and V_{CE} that exist in a transistor circuit when *no input signal is applied.*

It is also known as the *dc operating* point or *working point.* The best position for this point is midway between cut-off and saturation points where $V_{CE} = \frac{1}{2} V_{CC}$ (like point *D* in Fig. 20.1).

Example 20.1. *For the circuit shown in Fig. 20.2 (a), draw the dc load line and locate quiescent or dc working point.*

Solution. The cut-off point is easily found because it lies along *X*-axis where V_{CB} = 20 V *i.e.*, point *A* in Fig. 20.2 (*b*). At saturation point *B*, saturation value of collector current is

$$I_{C(sat)} = V_{CC}/R_L = 20/5 \text{ K} = 4 \text{ mA}$$

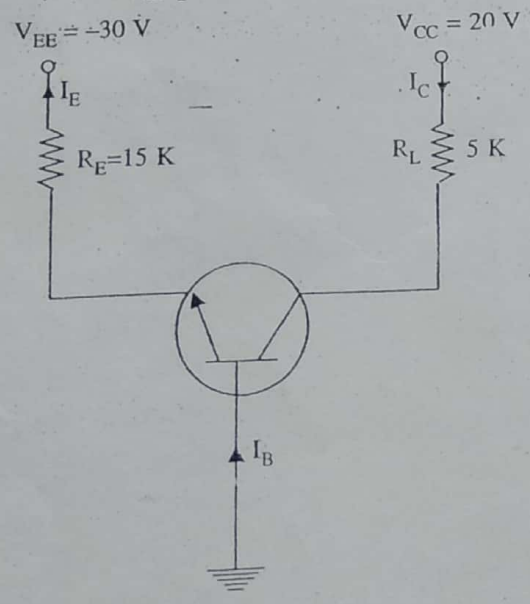
The line *AB* represents the load line for the given circuit.

We will now find the actual operating point.

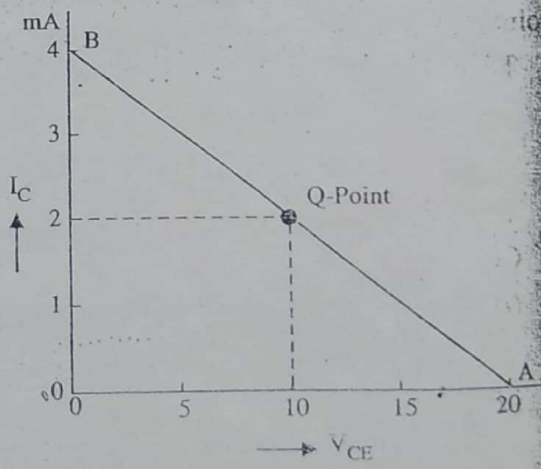
$$I_E = V_{EE}/R_E = 30/15 \text{ K} = 2 \text{ mA} \qquad \text{— neglecting}$$

$$I_C = \alpha I_E \cong I_E = 2 \text{ mA}; \qquad \therefore \quad V_{CB} = V_{CC} - I_C R_L = 20 - 2 \times 5 =$$

Hence, *Q*-point is located at **(10 V; 2 mA)** as shown in Fig. 20.2 (*b*).



(*a*)



(*b*)

Fig. 20.2

Example 20.2. *In the CB circuit of Fig. 20.3 (a), find*

(a) dc operating point and dc load line

(b) maximum peak-to-peak unclipped signal

(c) the approximate value of ac source voltage that will cause clipping.

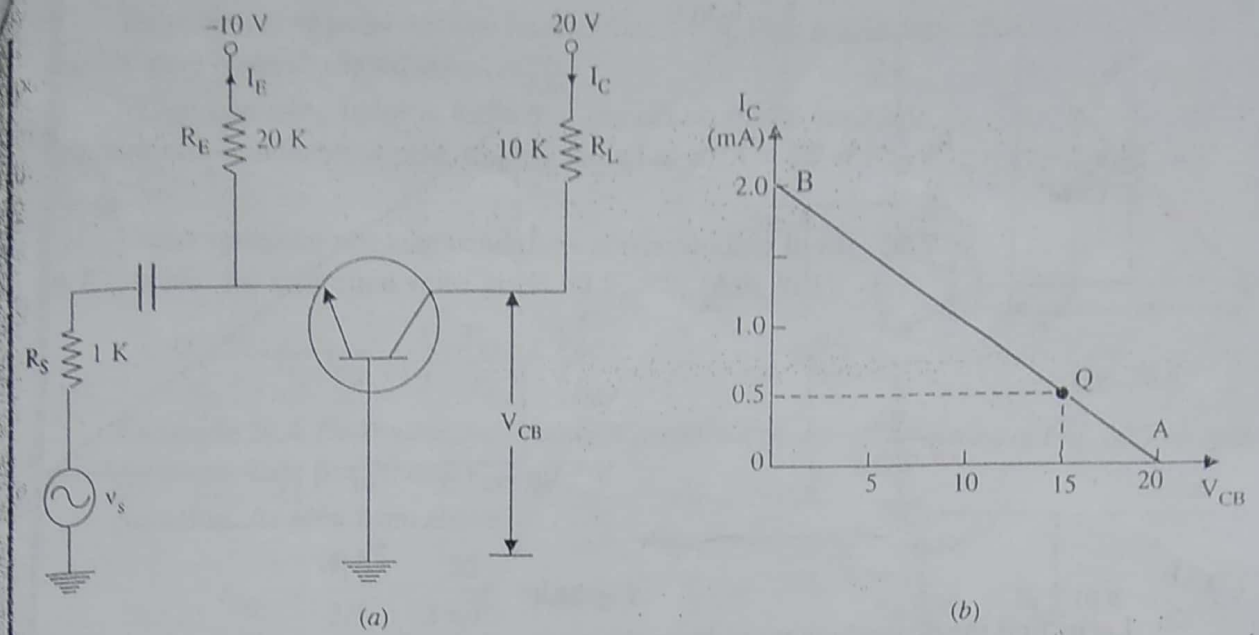


Fig. 20.3

Solution. (*a*) $I_{C\,(sat)} = \dfrac{V_{CC}}{R_L} = \dfrac{20}{10} = 2$ mA — point *B*

V_{CB} at cut-off $= V_{CC} = 20$ V — point *A*

Hence, *AB* is the dc load line and is shown in Fig. 20.3 (*b*).

Now, $I_E = 10/20 = 0.5$ mA ; $I_C \cong I_E = 0.5$ mA

$\therefore$ $V_{CB} = V_{CC} - I_C R_L = 20 - 0.5 \times 10 = 15$ V

The *Q*-point is located at **(15 V, 0.5 mA)**

(*b*) It is obvious from Fig. 20.3 (*b*) that maximum positive swing can be from 15 V to 20 V *i.e.*, 5 V only. Of course, on the negative swing, the output swing can go from 15 V down to zero volt. The limiting factor being *cut-off on positive half-cycle*, hence maximum unclipped peak-to-peak voltage that we can get from this circuit is $2 \times 5 =$ **10 V.**

(*c*) The approximate voltage gain of the above circuit is

$$= \frac{v_{out}}{v_s} = \frac{R_{ac}}{R_s} = \frac{10\text{ K}}{1\text{ K}} = 10$$

It means that signal voltage will be amplified 10 times. Hence, maximum value of source voltage for obtaining unclipped or undistorted output is

$$v_s = \frac{v_{out}}{10} = \frac{10\ V_{p-p}}{10} = 1\ V_{p-p}$$

Example 20.3. *For the CE circuit shown in Fig. 20.4 (a), draw the dc load line and mark the dc working point on it. Assume* $\beta = 100$ *and neglect* V_{BE}.

Solution. Cut-off point *A* is located where,

$I_C = 0$ and $V_{CE} = V_{CC} = 30$ V. Saturation point *B* is given where

$V_{CE} = 0$

and $I_{C(sat)} = 30/5$ K $= 6$ mA.

Line *AB* represents the load line in Fig. 20.4 (*b*).

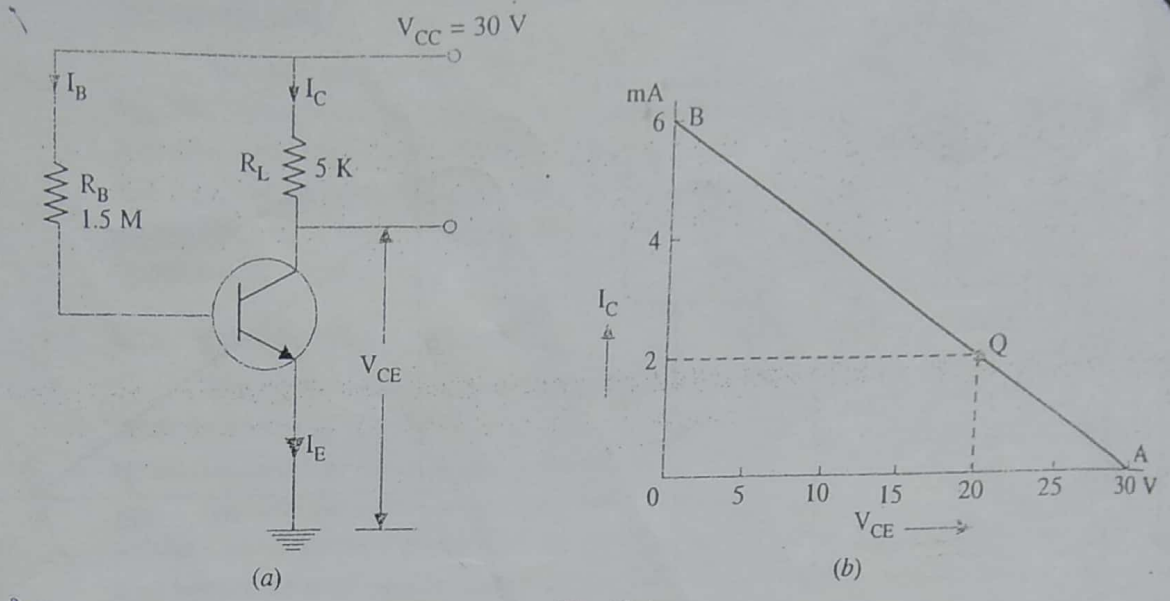


Fig. 20.4

Let us find the dc working point from the given values of resistances and supply voltage.

$$I_B = 30/1.5\ \text{M} = 20\ \mu\text{A};\quad I_C = \beta I_B = 100 \times 20 = 2000\ \mu\text{A} = 2\ \text{mA};$$

$$V_{CE} = V_{CC} - I_C R_L = 30 - 2 \times 5 = 20\ \text{V}$$

Hence, Q-point is **(20 V; 2 mA)** as shown in Fig. 20.4. (*b*).

20.2. Q-point and Maximum Undistorted Output

Position of the Q-point on the dc load line determines the maximum signal that we can get from the circuit before clipping occurs. Consider the cases shown in Fig. 20.5.

In Fig. 20.5 (*a*), when Q, is located near cut-off point, signal first starts to clip at A. It is called *cut-off clipping* because the positive swing of the signal drives the transistor to cut-off. In fact, as seen from Fig. 20.5 (*a*), maximum positive swing is $= I_{CQ} R_{ac}$.

If the Q-point Q_2 is located near saturation point, then clipping first starts at point B as shown in Fig. 20.5 (*b*). It is caused by saturation. The maximum negative swing $= V_{CEQ}$.

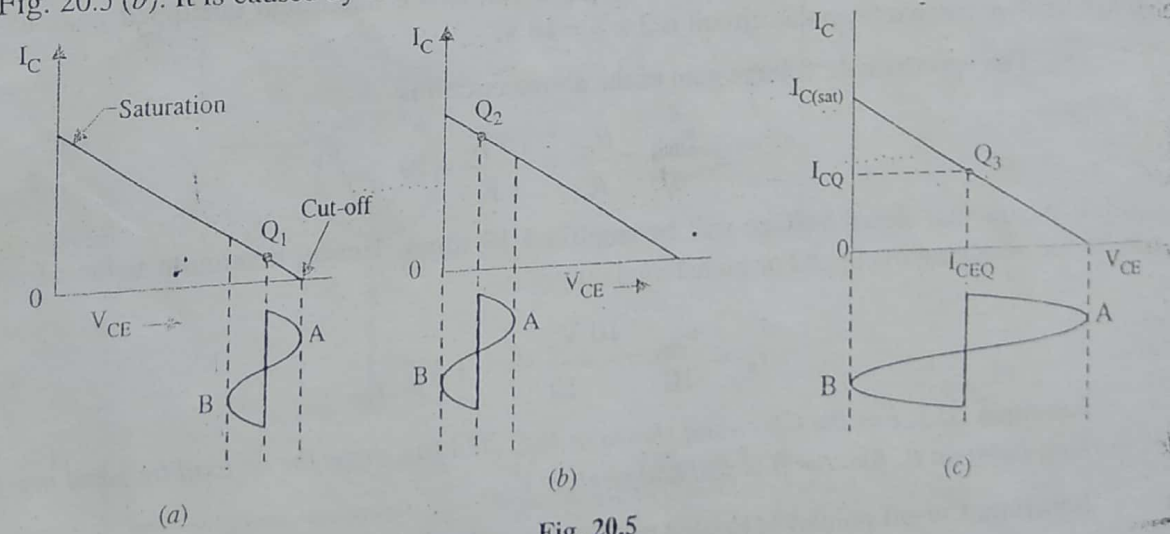


Fig. 20.5

In Fig. 20.5 (*c*), the Q-point Q_3 is located at the *centre* of the load line. In this condition, we get the *maximum possible output signal*. The point Q_3 gives the *optimum* Q-point. The maximum undistorted signal $= 2V_{CEQ}$.

In general, consider the case shown in Fig. 20.6. Since $A < B$, maximum possible peak-to-peak output signal $= 2A$.

If the operating point were so located that $A > B$, then maximum possible peak-to-peak output signal = $2B$.

When operating point is located at the centre of the load line, then maximum undistorted peak-to-peak signal is = $2A = 2B = V_{CC} = V_{CEQ}$.

Under optimum working conditions corresponding to Fig. 20.5 (c), I_{CQ} is half the saturation value given by V_{CC}/R_L (Art. 20.1).

$$\therefore \quad I_{CQ} = \frac{1}{2} \cdot \frac{V_{CC}}{R_L} = \frac{V_{CC}}{2R_L}$$

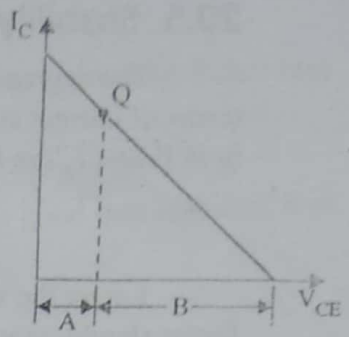


Fig. 20.6

Example 20.4. *Determine the value of R_B required to adjust the circuit of Fig. 20.7 to optimum operating point. Take $\beta = 50$ and $V_{BE} = 0.7$ V.*

Solution. As seen from above

$$I_{CQ} = \frac{V_{CC}}{2R_L} = \frac{20}{2 \times 10} = 1 \text{ mA}$$

The corresponding base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1}{50} = 20 \ \mu\text{A}$$

Now, $V_{CC} = I_B R_B + V_{BE}$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7}{20 \times 10^{-6}} = 965 \text{ K}$$

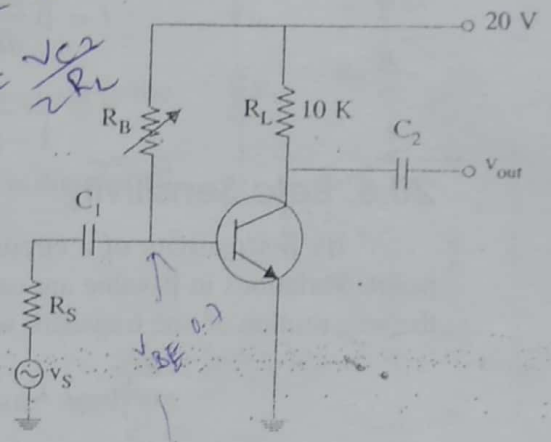


Fig. 20.7

20.3. Need for Biasing a Transistor

For normal operation of a transistor amplifier circuit, it is essential that there should be a

(*a*) forward bias on the emitter-base junction, and

(*b*) reverse bias on the collector-base junction.

In addition, *amount* of bias required is important for establishing the Q-point which is dictated by the mode of operation desired.

If the transistor is not biased correctly, it would

1. work inefficiently and 2. produce distortion in the output signal.

It is desirable that once selected, the Q-point should remain stable *i.e.*, should not shift its position due to temperature rise etc. Unfortunately, this does not happen in practice unless special efforts are made for the purpose.

20.4. Factors Affecting Bias Variations

In practice, it is found that even after careful selection, Q-point tends to shift its position.

This bias instability is the direct result of thermal instability which itself is produced by cumulative increase in I_C that may, if unchecked, lead to thermal runaway (Art. 19.13).

The collector current for CE circuit is given by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO}$$

This equation has three variables : β, I_B and I_{CO} all of which are found to increase with temperature. In particular, increase in I_{CO} produces significant increase in collector current I_C. This leads to increased power dissipation with further increase in temperature and hence I_C. Being a cumulative process, it can lead to thermal runaway which will destroy the transistor itself !

However, if by some circuit modification, I_C is made to decrease with temperature automatically, then decrease in the term βI_B can be made to neutralize the increase in the term $(1 + \beta) I_{CO}$, thereby keeping I_C constant. This will achieve thermal stability resulting in bias stability.

20.5. Stability Factor

The degree of success achieved in stabilizing I_C in the face of variations in I_{CO} is expressed in terms of current stability factor S. It is defined as the *rate of change of* I_C *with respect to* I_{CO} *when both* β *and* I_B *are held constant.*

$$\therefore \qquad S = \frac{d I_C}{d I_{CO}} \qquad \text{— } I_B \text{ constant}$$

Larger the value of S, greater the thermal instability and *vice versa* (in view of the above, this factor should, more appropriately, be called instability factor).

The stability factor may be alternatively expressed by using the well-known equation $I_C = \beta I_B + (I + \beta) I_{CO}$ which, on differentiation with respect to I_C, yields.

$$I = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C} = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{1}{S}$$

$$\therefore \qquad S = \frac{(1 + \beta)}{1 - \beta \, (dI_B / dI_C)}$$

20.6. Beta Sensitivity

By β-sensitivity of a circuit is meant the influence that the β-value has on its dc operating point. Variations in β-value are caused either by variations in the circuit operating conditions or by the substitution of one transistor with another. Beta sensitivity K_β is given by

$$\frac{dI_C}{I_C} = K_\beta \frac{dI_B}{\beta} \qquad \text{or} \qquad K_\beta = \frac{\beta}{I_C} \cdot \frac{dI_C}{d_B}$$

Obviously, K_β is dimensionless ratio and can have values ranging from zero to unity.

20.7. Stability Factor for CB and CE Circuits

(*i*) CB Circuit

Here, collector current is given by

$$I_C = \alpha I_E + I_{CO} \qquad \text{— Art. 18.12}$$

$$\therefore \qquad \frac{dI_C}{dI_{CO}} = 0 + 1 \qquad \therefore \quad S = 1$$

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(*ii*) CE Circuit

$$I_C = \beta I_B + (I + \beta) I_{CO} \qquad \text{— Art. 18.13}$$

$$\therefore \qquad \frac{dI_C}{dI_{CO}} = (1 + \beta) \qquad \text{— treating } I_B \text{ as a constant}$$

$$\therefore \qquad S = (1 + \beta).$$

If $\beta = 100$, then $S = 101$

which means that I_C changes 101 times as much as I_{CO}.

20.8. Different Methods for Transistor Biasing

Some of the methods used for providing bias for a transistor are :

1. Base bias or fixed current bias (Fig. 19.14)

It is not a very satisfactory method because bias voltages and currents do not remain constant during transistor operation.

2. Base bias with emitter feedback (Fig. 20.7)

This circuit achieves good stability of dc operating point against changes in β with the help of emitter resistor which causes degeneration to take place.

3. Base bias with collector feedback (Fig. 20.9)

It is also known as collector-to-base bias or collector feedback bias. It provides better bias stability.

4. Voltage divider bias (Fig. 20.10)

It is most widely used in linear discrete circuits because it provides good bias stability. It is also called universal bias circuit or base bias with one supply.

Each of the above circuits will now be discussed separately.

20.9. Base Bias

It has already been discussed in Art. 19.17 and is shown in Fig. 19.44. For such a circuit, $S = 1$ and $K\beta = 1$.

20.10. Base Bias with Emitter Feedback

This circuit is obtained by simply adding an emitter resistor to the base bias circuit as shown in Fig. 20.8.

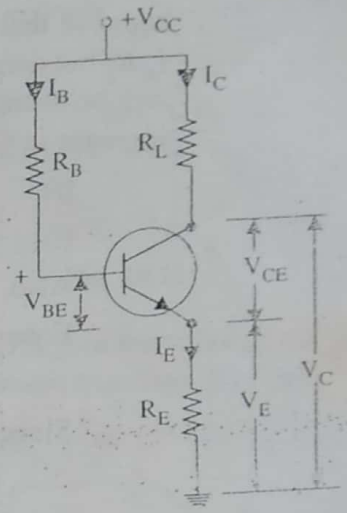

Fig. 20.8

1. At saturation, V_{CE} is essentially zero, hence V_{CC} is distributed over R_L and R_E.

$$\therefore \qquad I_{C(sat)} = \frac{V_{CC}}{R_E + R_L}$$

2. I_C can be found as follows :

Consider the supply, base, emitter and ground route. Applying Kirchhoff's Voltage Law, we have

$$-I_B R_B - V_{BE} - I_E R_E + V_{CC} = 0 \qquad ...(i)$$

or $$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

Now $$I_B = I_C/\beta \qquad \text{and} \qquad I_E \cong I_C$$

Substituting these values in the above equation, we have

$$V_{CC} \cong \frac{I_C R_B}{\beta} + V_{BE} + I_C R_E$$

$$\therefore \qquad I_C \cong \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta} \cong \frac{V_{CC}}{R_E + R_B/\beta} \qquad \text{— neglecting } V_{BE}$$

(we could have applied the β-rule given in Art. 19.11)

3. collector-to-ground voltage $\qquad V_C = V_{CC} - I_C R_L$

4. emitter-to-ground voltage $\qquad V_E = I_E R_E \cong I_C R_E$

The β-sensitivity of this circuit is $K_\beta = \dfrac{1}{1 + \beta R_E / R_B}$

Example 20.5. *For the circuit shown in Fig. 20.9, find (i) $I_{C(sat)}$, (ii) I_C, (iii) V_C, (iv) V_E, (v) V_{CE} and (vi) K_β.*

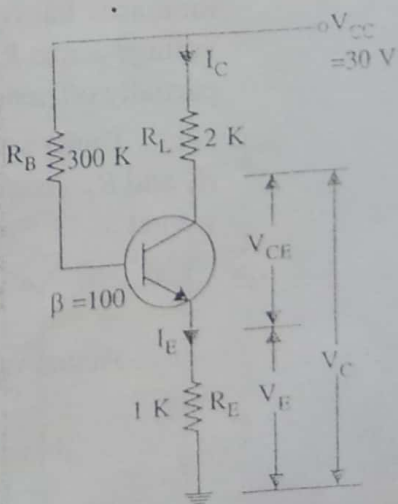

Fig. 20.9

Solution. (i) $I_{C(sat)} = \dfrac{V_{CC}}{R_E + R_L} = \dfrac{30}{1+2} = \mathbf{10\ mA}$

(ii) actual $I_C \cong \dfrac{V_{CC}}{R_E + R_B/\beta} = \dfrac{30}{1 + 300/100} = \mathbf{7.5\ mA}$

(iii) $V_C = V_{CC} - I_C R_L = 30 - 7.5 \times 2 = \mathbf{15\ V}$

(iv) $V_E \cong I_E R_E \cong I_C R_E = 7.5 \times 1 = \mathbf{7.5\ V}$

(v) $$V_{CE} = V_C - V_E = 15 - 7.5 = 7.5 \text{ V}$$

(vi) $$K_\beta = \frac{1}{1 + 100 \times 1/300} = 0.75$$

20.11. Base Bias with Collector Feedback

This circuit (Fig. 20.10) is like the base bias circuit except that base resistor is returned to *collector* rather than to the V_{CC} supply. It derives its name from the fact that since voltage for R_B is derived from collector, there exists a negative feedback effect which tends to stabilise I_C against changes in β. To understand this action, suppose that somehow β increases. It will increase I_C as well as $I_C R_L$ but decrease V_C which is applied across R_B. Consequently, I_B will be decreased which will partially compensate for the original increase in β.

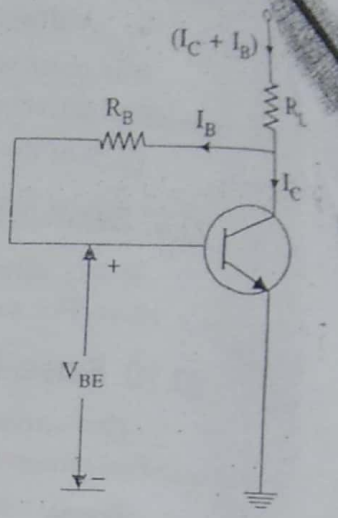

Fig. 20.10

(i) $$I_{C(sat)} = V_{CC} / R_L \qquad \text{— since } V_{CE} = 0$$

(ii) $$V_C = V_{CC} - (I_B + I_C) R_L \cong V_{CC} - I_C R_L$$

Also, $$V_C = I_B R_B + V_{BE}$$

Equating the two expressions for V_C, we have

$$I_B R_B + V_{BE} \cong V_{CC} - I_C R_L$$

Since $I_B = I_C/\beta$, we get

$$\frac{I_C}{\beta} R_B + V_{BE} \cong V_{CC} - I_C R_L$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_L + R_B/\beta} \cong \frac{V_{CC}}{R_L + R_B/\beta}$$

This is also the approximate value of I_E (again, we could take the help of β-rule).

$$K_\beta = \frac{1}{1 + \beta R_L / R_B} = 1 - \frac{I_C}{I_{C(sat)}}$$

20.12. Base Bias with Collector and Emitter Feedbacks

In the circuit of Fig. 20.11, both collector and emitter feedbacks have been used in an attempt to reduce circuit sensitivity to changes in β. If β increases, emitter voltage increases but collector voltage decreases. It means that voltage across R_B is reduced causing I_B to decrease thereby partially off-setting the increase in β.

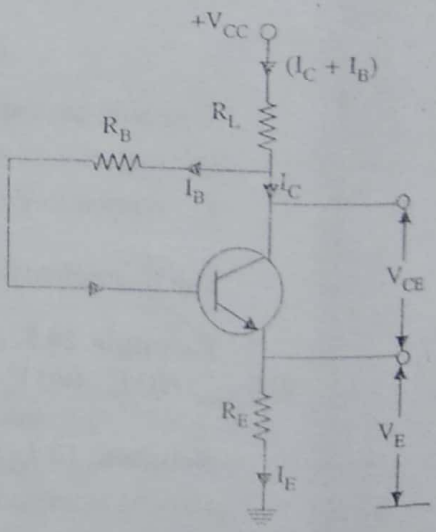

Fig. 20.11

Under saturation conditions, V_{CC} is distributed over R_L and R_E. Assuming I_B to be negligible as compared to I_C, we get

$$I_{C(sat)} = V_{CC}/(R_E + R_L).$$

Actual value of I_C is $I_C \cong \dfrac{V_{CC} - V_{BE}}{R_E + R_L + R_B/\beta}$

— going via R_B because V_{CE} is unknown

$$V_C = V_{CC} - (I_C + I_B) R_L \; ; \cong V_{CC} - I_C R_L$$

$$V_E = I_E R_E \cong I_C R_E \; ; \; V_{CE} = V_C - V_E$$

$$V_{CE} \cong V_{CC} - I_C (R_L + R_E)$$

It can be proved that

$$K_\beta = \frac{1}{1 + \beta\,(R_E + R_L)/R_B} = 1 - \frac{I_C}{I_{C(sat)}}$$

Obviously, K_β will be degraded with increase in R_B.

Example 20.6. *For the circuit shown in Fig. 20.12, find (a) $I_{C(sat)}$ (b) V_{CE} and (c) K_β. Neglect V_{BE} and take $\beta = 100$.*

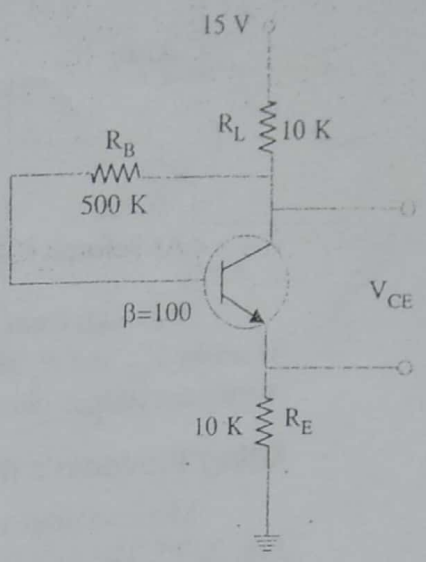

Fig. 20.12

Solution. (*a*) $I_{C(sat)} = 15/(10 + 10) = \mathbf{0.75\ mA}$

(*b*) $$I_C = \frac{V_{CC}}{R_E + R_L + R_B/\beta} = \frac{15}{10 + 10 + 500/100}$$

$$= \mathbf{0.6\ mA}$$

$$V_{CE} = 15 - 0.6\,(10 + 10) = 3\ \text{V}$$

(*c*) $$K_\beta = \frac{1}{1 + 100\,(10 + 10)/50} = \mathbf{0.2}$$

or $$K_\beta = 1 - I_C/I_{C(sat)} = 1 - 0.6/0.75 = \mathbf{0.2}$$

Obviously, K_β will be degraded with increase in R_B.

Example 20.7. *For the transistor amplifier circuit shown in Fig. 20.13, find the value of the collector bias of voltage V_C. Also, find the new value of R_B so that the maximum transistor β of 300 brings V_C down to 5 volt.*

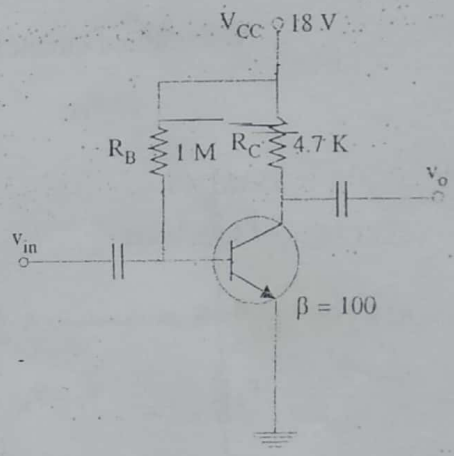

Fig. 20.13

Solution. $I_B = (18 - 0.7)\ \text{V}/1\ \text{M} = 17.3\ \mu\text{A}$

$I_C = \beta I_B = 100 \times 17.3 = 1.73\ \text{mA}$

$V_{RC} = I_C R_C = 1.73\ \text{mA} \times 4.7\ \text{K} = 8.1\ \text{V}$

$\therefore\quad V_C = V_{CC} - V_{RC} = 18 - 8.1 = \mathbf{9.9\ V}$

Since, now $V_C = 5$ V, hence drop across the collector load resistor is given by

$V_{RC} = V_{CC} - V_C = 18 - 5 = 13\ \text{V}$

$\therefore\quad I_C = 13\ \text{V}/4.7\ \text{K} = 2.8\ \text{mA}$

$I_B = I_C/\beta = 2.8\ \text{mA}/300 = 9.2\ \mu\text{A}$

$V_{RB} = V_{CC} - V_{BE} = 18 - 0.7 = 17.3\ \text{V}$

$\therefore$ new value of $R_B = 17.3\ \text{V}/9.2\ \mu\text{A} = \mathbf{1.9\ M}$

20.13. Voltage Divider Bias

This arrangement is commonly used for transistors incorporated in integrated circuits (ICs).

The name 'voltage divider' is derived from the fact that resistors R_1 and R_2 form a potential divider across V_{CC} (Fig. 20.14)*. The voltage drop V_2 across R_2 forward-biases the emitter whereas V_{CC} supply reverse biases the collector.

As per voltage divider theorem,

$$V_2 = V_{CC} \cdot R_2/(R_1 + R_2)$$

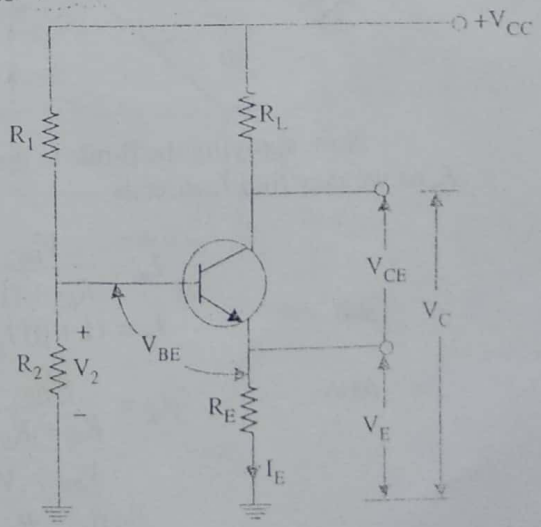

Fig. 20.14

* It is also known as Universal Bias Stabilization Circuit.

As seen, $V_E = V_2 - V_{BE}$

$$\therefore \quad I_E = \frac{V_E}{R_E} = \frac{V_2 - V_{BE}}{R_E} \cong \frac{V_2}{R_E}$$

Also, $V_C = V_{CC} - I_C R_L$

$$V_{CE} = V_C - V_E = V_{CC} - I_C R_L - I_E R_E$$
$$\cong V_{CC} - I_C (R_L + R_E) \qquad \therefore \quad I_C \cong I_E$$

As before, $I_{C(sat)} \cong \dfrac{V_{CC}}{R_L + R_E}$; $\qquad K_\beta = \dfrac{1}{1 + \beta R_E / (R_1 \parallel R_2)}$

It is seen from above calculations that value of β was never used anywhere. The base voltage is set by V_{CC} and R_1 and R_2. The dc bias circuit is independent of transistor β. That is why it is such a very popular bias circuit.

Using Thevenin's Theorem

More accurate results can be obtained by Thevenizing the voltage divider circuit as shown in Fig. 20.15. The first step is to open the base lead at point A and remove the transistor along with R_L and R_E, thereby leaving the voltage divider circuit behind as in Fig. 20.15 (*a*) and (*b*).

$$V_{th} = V_2 = V_{CC} \cdot \frac{R_2}{R_1 + R_2} \quad \text{and} \quad R_{th} = R_1 \parallel R_2 = \frac{R_1 R_2}{(R_1 + R_2)}$$

The original circuit is reduced to that shown in Fig. 20.15 (*c*) where $V_{th} = V_{BB'}$ and $R_{th} = R_{B'}$.

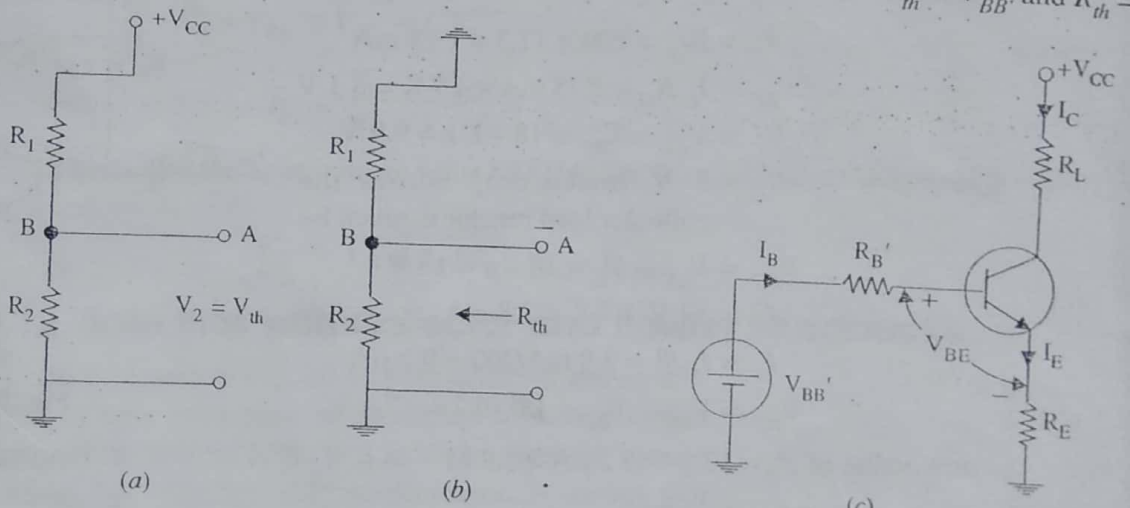

Fig. 20.15

Now, applying the β-rule to the circuit of Fig. 20.15 (*b*), we may find I_B and then $I_E = (1 + \beta) I_B$ or we may find I_E directly.

$$I_B = \frac{V_{BB'} - V_{BE}}{R_{B'} + (1 + \beta) R_E} \cong \frac{V_{BB'} - V_{BE}}{R_{B'} + \beta R_E} = \frac{V_{BB'}}{R_{B'} + \beta R_E}$$

and $I_E = (1 + \beta) I_B$

Also $$I_E = \frac{V_{BB'} - V_{BE}}{R_E + R_{B'} / (1 + \beta)}$$

$$\cong \frac{V_{BB'} - V_{BE}}{R_E + R_{B'} / \beta} \cong \frac{V_{BB'}}{R_E + R_{B'} / \beta}$$

$\therefore$ $V_{CE} = V_{CC} - I_C R_L - I_E R_E$

$= V_{CC} - I_C (R_L + R_E)$

Example. 20.8. *For the circuit of Fig. 20.16, find (a) $I_{C(sat)}$, (b) I_C, (c) V_{CE}, (d) K_β. Neglect V_{BE} and take $\beta = 50$.*

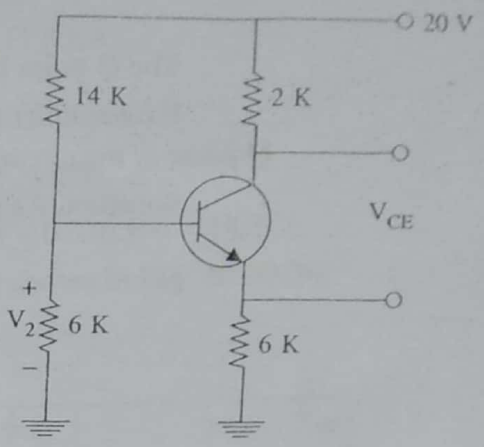

Fig. 20.16

Solution. (a) $I_{C(sat)} = \dfrac{V_{CC}}{R_L + R_E} = \dfrac{20}{2+6} = \mathbf{2.5\ mA}$

(b) $I_C \cong I_E \cong V_2 / R_E = 6/6 = \mathbf{1\ mA}$

(c) $V_{CE} = V_{CC} - I_C (R_L + R_E)$

$= 20 - 1\,(2+6) = \mathbf{12\ V}$

(d) $R_1 \parallel R_2 = 84/20 = 4.2\ \text{K}$

$\therefore \quad K_\beta = \dfrac{1}{1 + 50 \times 6/4.2} = \mathbf{0.0138}$

Example 20.9. *Calculate the emitter bias current for the transistor amplifier circuit shown in Fig. 20.17.*

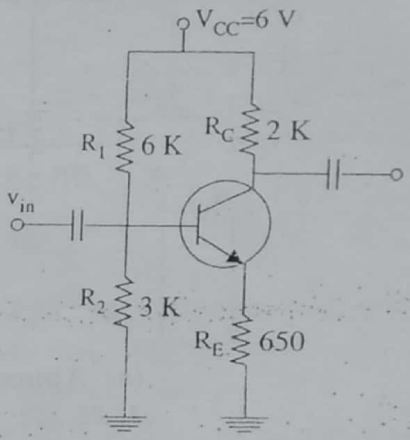

Fig. 20.17

Solution. Let us first find the value of base voltage.

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = 6 \cdot \frac{3}{3+6} = 2\ \text{V}$$

$$V_E = V_B - 0.7 = 2 - 0.7 = 1.3\ \text{V}$$

$$\therefore \quad I_E = V_E / R_E = 1.3/650 = \mathbf{2\ mA}$$

Example 20.10. *For the circuit shown in Fig. 20.18 (a), draw the dc load line and mark in the Q-point of the circuit. Assume silicon transistor.*

Solution. Under cut-off condition ; $V_{CE} = V_{CC}$

$$\therefore \quad V_{CE(cut\text{-}off)} = V_{CC} = 20\ \text{V} \quad \text{— point } A \text{ in Fig. 20.18 } (b)$$

$$I_{C(sat)} = \frac{V_{CC}}{R_L + R_E} = \frac{20}{2+3} = 4\ \text{mA} \quad \text{— point } B \text{ in Fig. 20.18 } (b)$$

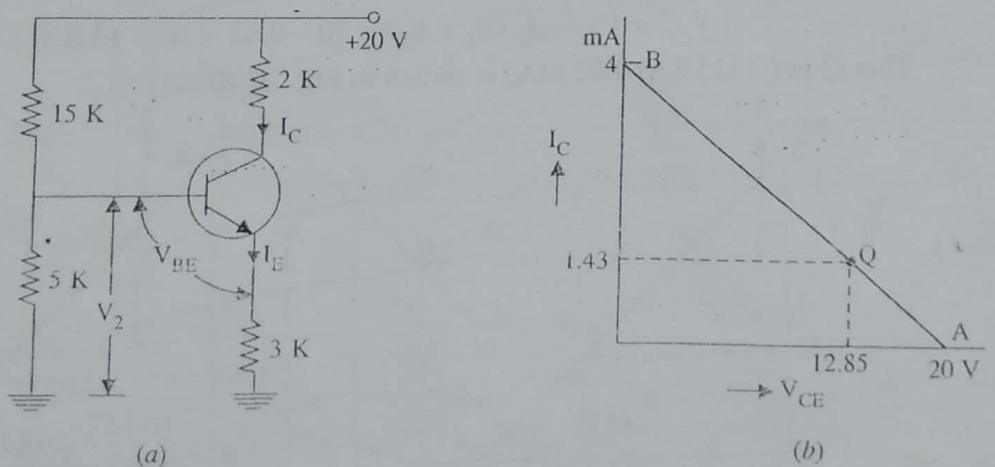

Fig. 20.18

$$V_2 = V_{CC} \frac{R_2}{R_1 + R_2} = 20 \times \frac{5}{15+5} = 5\ \text{V}$$

$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{3} = 1.43\ \text{mA}$$

Now, $\quad I_C \cong I_E = 1.43\ \text{mA}$

$$V_{CE} = V_{CC} - I_C (R_L + R_E)$$
$$= 20 - 1.43\ (2 + 3) = \mathbf{12.85\ V}$$

The Q-point is shown in Fig. 20.18 (b).

Example 20.11. *For the circuit shown in Fig. 20.19 (a), draw the dc load line and Q-point of the circuit. Assume germanium material with $V_{BE} = 0.3$ V and $\beta = 50$.*

Solution. As usual.

$$V_{CE(cut\text{-}off)} = V_{CC} = 20\ \text{V} \quad \text{— point } A \text{ in Fig. 2}$$

$$I_{C(sat)} = \frac{V_{CC}}{R_L + R_E} = \frac{20}{4 + 6} = 2\ \text{mA} \quad \text{— point } B \text{ in Fig. 20}$$

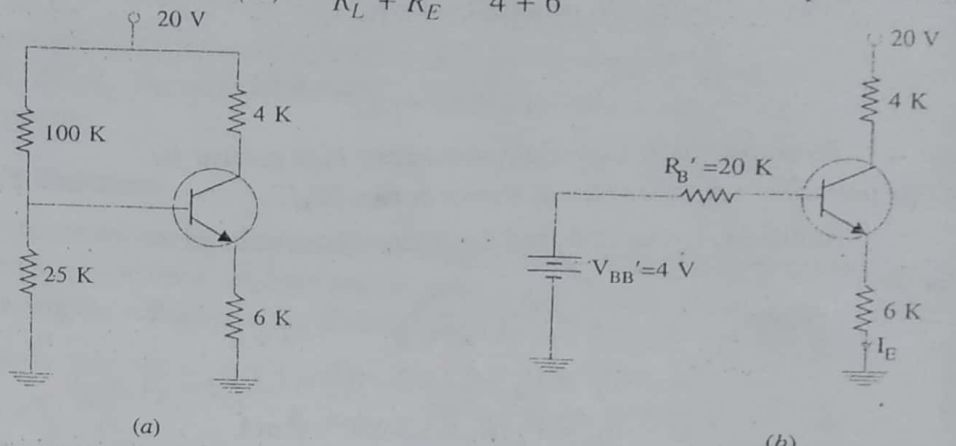

Fig. 20.19

(a) Approximate Method

$$V_2 = V_{CC} \frac{R_2}{R_1 + R_2} = 20 \times \frac{25}{125} = 4\ \text{V}$$

$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{4 - 0.3}{6} = 0.62\ \text{mA}$$

Also, $I_C \cong I_E = 0.62$ mA

$\therefore$ $V_{CE} = V_{CC} - I_C (R_L + R_E) = 20 - 0.62 \times 10 = \mathbf{13.8\ V}$

This Q-point (**13.8 V, 0.62 mA**) is shown in Fig. 20.20 (a).

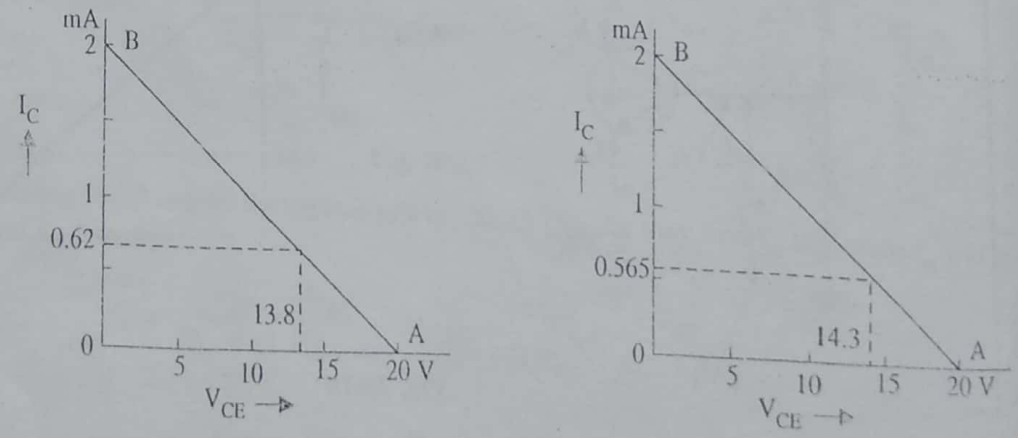

Fig. 20.20

(b) Accurate Method

As seen from Fig. 20.19 (b)

$$V_{BB'} = 20 \times 25 / 125 = 4\ \text{V}$$

$$I_B = \frac{V_{BB'} - V_{BE}}{R_{B'} + (1 + \beta)\, R_E} = \frac{4 - 0.3}{20 + 51 \times 6} = 11.3\ \mu A$$

$$I_C = \beta I_B = 50 \times 11.3 = 565\ \mu A \qquad = 0.565\ mA$$

$$I_E = (1 + \beta)\, I_B = 576\ \mu A = 0.576\ mA$$

$$\therefore \qquad V_{CE} = V_{CC} - I_C R_L - I_E R_E = 20 - 0.565 \times 4 - 0.576 \times 6 = \mathbf{14.3\ V}$$

The new and more accurate Q-point (**14.3 V, 0.565 mA**) is shown in Fig. 20.20 (*b*).

20.14. Load Line and Output Characteristics

In order to study the effect of bias conditions on the performance of a *CE* circuit, it is necessary to superimpose the dc load line on the transistor output (V_{CE}/I_C) characteristics. Consider a silicon *NPN* transistor which is connected in *CE* configuration (Fig. 20.21) and whose output characteristics are given in Fig. 20.22. Let its $\beta = 100$.

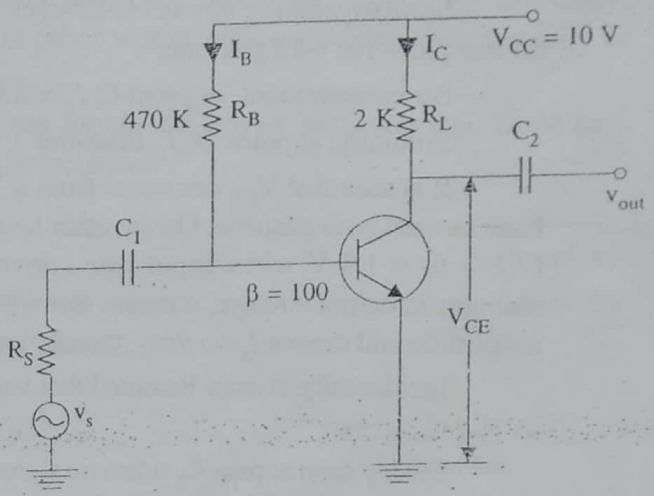

Fig. 20.21

First, let us find the cut-off and saturation points for drawing the dc load line and then mark in the Q-point.

$I_{C(sat)} = 10/2 = 5$ mA
— point B in Fig. 20.22

$V_{CE(cut\text{-}off)} = V_{CC} = 10$ V
— point A in Fig. 20.22

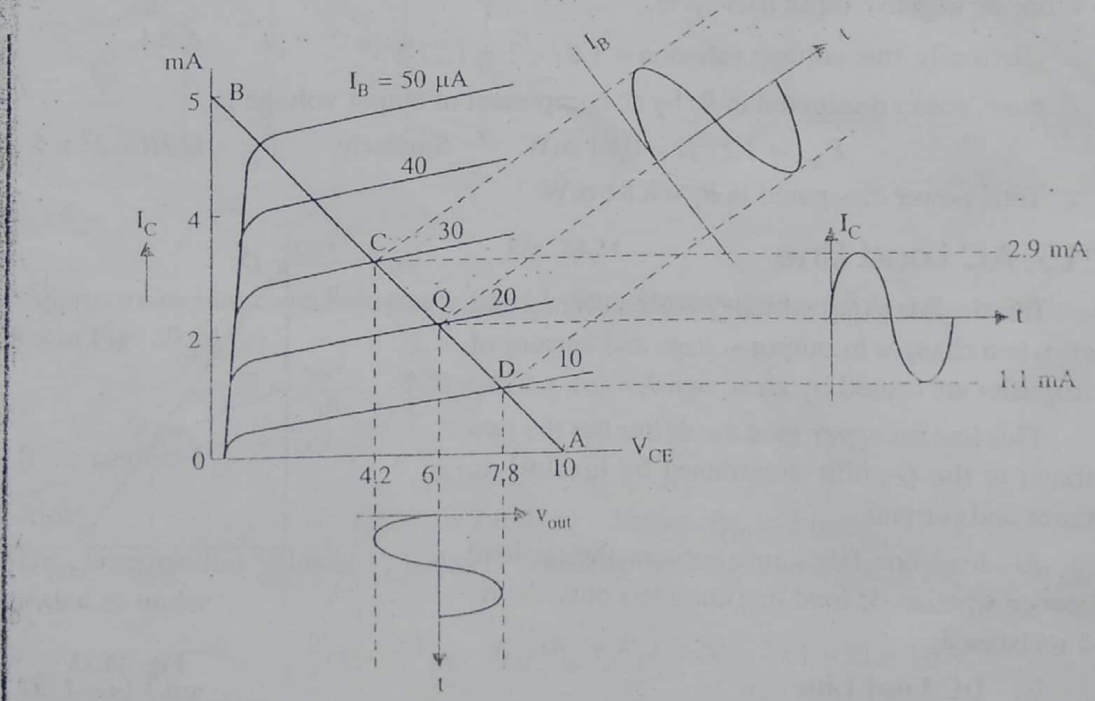

Fig. 20.22

The load line is drawn in Fig. 20.22.

Actual $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{470} = 20\ \mu A$$

$$I_C = \beta I_B = 100 \times 20 = 2000\ \mu A$$
$$= 2\ mA$$
$$V_{CE} = V_{CC} - I_C R_L = 10 - 2 \times 2 = 6\ V$$

This locates the Q-point in Fig. 20.22.

Suppose an ac input signal voltage injects a sinusoidal base current of peak value 10 μA the circuit of Fig. 20.21. Obviously, it will swing the operating or Q-point up and down along the line.

When positive half-cycle of I_B is applied, the Q-point shifts to point C which lies on $(20 + 10) = 30\ \mu A$ line.

Similarly, during negative half-cycle of input base current, Q-point shifts to point D which on the $(20 - 10) = 10\ \mu A$ line.

By measurement, at point C, $I_C = 2.9$ mA. Hence, $V_{CE} = 10 - 2 \times 2.9 = 4.2$ V

Similarly, at point D, I_C measures 1.1 mA. Hence, $V_{CE} = 10 - 2 \times 1.1 = 7.8$ V

It is seen that V_{CE} decreases from 6 V to 4.2 V *i.e.*, by a peak value of $(6 - 4.2) = 1.8$ V wh base current goes positive. On the other hand, V_{CE} increases from 6 V to 7.8 V *i.e.*, by a peak value $(7.8 - 6) = 1.8$ V when input base current signal goes negative. Since changes in V_{CE} repres changes in output voltage, it means that when input signal is applied, I_B varies according to the sig amplitude and causes I_C to vary, thereby producing voltage variations.

Incidentally, it may be noted that variations in voltage drop across R_L are exactly the same in V_{CE}.

Steady drop across R_L when no signal is applied $= 2 \times 2 = 4$ V. When base signal goes positiv drop across $R_L = 2 \times 2.9 = 5.8$ V. When base signal goes negative, $I_C = 1.1$ mA and drop across R_L $2 \times 1.1 = 2.2$ V.

Hence, voltage variation is $= 5.8 - 4 = 1.8$ V during positive input half-cycle and $4 - 2.2 = 1.8$ V during negative input half-cycle.

Obviously, rms voltage variation $= 1.8/\sqrt{2} = 1.27$ V

Now, power dissipated in R_L by ac component of output voltage is

$$P_{ac} = 1.27^2/2 = 0.81\ mW. \quad \text{Similarly,} \quad P_{dc} = I_C^2 R = 2^2 \times 2 = 8\ mW$$

Total power dissipated in $R_L = 8.81$ mW.

20.15. AC Load Line

It is the line along which Q-point shifts up and down when changes in output voltage and current of an amplifier are caused by an ac signal.

This line is *steeper than the dc line* but the two intersect at the Q-point determined by biasing dc voltages and currents.

AC load line takes into account the ac load resistance whereas dc load line considers only the dc load resistance.

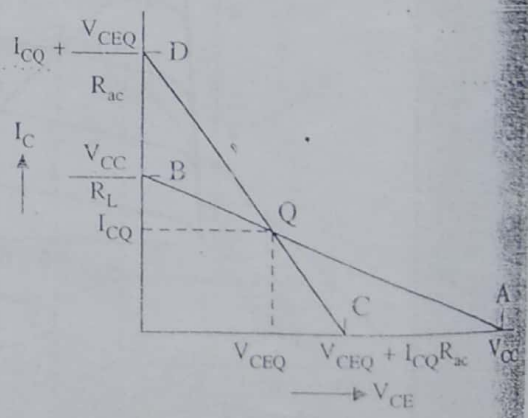

Fig. 20.23

(i) DC Load Line

The cut-off point for this line is where $V_{CE} = V_{CC}$.

It is also written as $V_{CE(cut\text{-}off)}$.

Saturation point is given by

$I_C = V_{CC}/R_L$. It is also written as $I_{C(sat)}$.

It is represented by straight line AQB in Fig. 20.23.

(ii) AC Load Line

The cut-off point is given by $V_{CE(cut\text{-}off)} = V_{CEQ} + I_{CQ} R_{ac}$ where R_{ac} is the *ac load resistance**.

Saturation point is given by

$$I_{C(sat)} = I_{CQ} + V_{CEQ}/R_{ac}.$$ — as shown in Fig. 20.23

It is represented by straight line CQD in Fig. 20.23.

The slope of the ac load line is given by $y = -1/R_{ac}$.

It is seen from Fig. 20.23 that maximum possible positive signal swing is $= I_{CQ} R_{ac}$. Similarly, maximum possible negative signal swing is V_{CEQ}. In other words, peak-signal handling capacity is limited to $I_{CQ} R_{ac}$ or V_{CEQ} whichever is smaller.

Example 20.12. *Draw the dc and ac load lines for the CE circuit shown in Fig. 20.24 (a). What is the maximum peak-to-peak signal that can be obtained ?*

Solution. DC Load Line [Fig. 20.24 (*b*)]

$$V_{CE(cut\text{-}off)} = V_{CC} = 20 \text{ V}$$ — (point A)

$$I_{C(sat)} = V_{CC}/(R_L + R_E) = 20/5 = 4 \text{ mA}$$ — (point B)

Hence, AB represents dc load line for the given circuit.

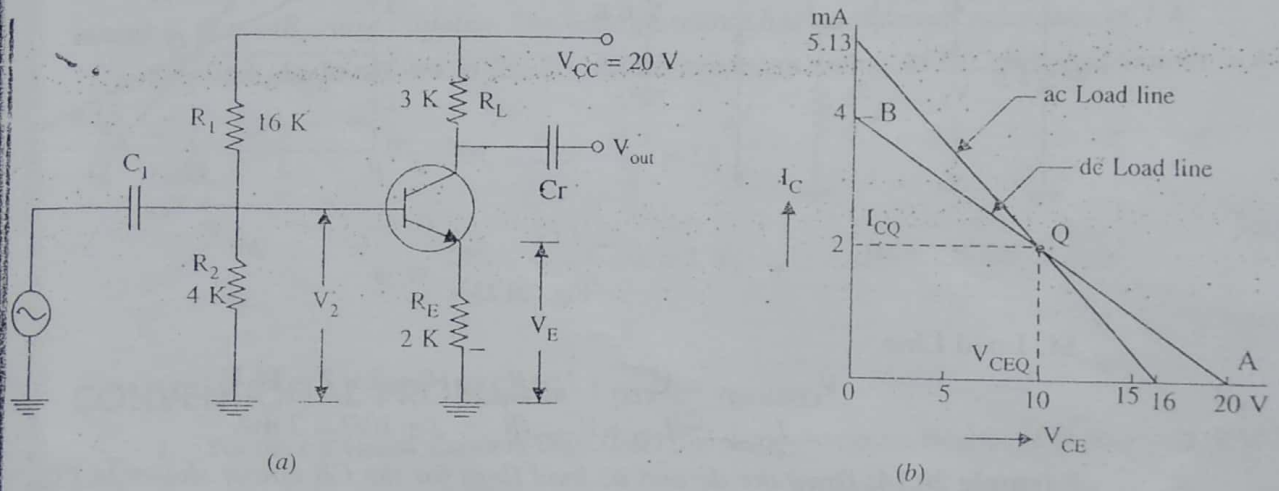

Fig. 20.24

Approximate bias conditions can be quickly found by assuming that I_B is too small to affect the base bias in Fig. 20.24 (*a*).

$$V_2 = 20 \times 4/(4 + 16) = 4 \text{ V}$$

If we neglect V_{BE}, $\quad V_2 = V_E; \quad I_E = \dfrac{V_E}{R_E} = \dfrac{V_2}{R_E} = \dfrac{4}{2} = 2 \text{ mA}$

Also, $\quad I_C \equiv I_E = 2 \text{ mA}.$ $\quad$ Hence, $I_{CQ} = 2 \text{ mA}.$

The corresponding value of V_{CEQ} can be found by drawing dotted line in Fig. 20.24 (*b*) or may be calculated as under :

$$V_{CEQ} = V_{CC} - I_{CQ}(R_L + R_E) = 20 - 2(3 + 2) = 10 \text{ V}$$

AC Load Line

Cut-off point,

$$V_{CE(cut\text{-}off)} = V_{CEQ} + I_{CQ} R_{ac}$$

* Written as r_L in Chapter 21 (Art. 21.4)

Now, for the given circuit, ac load resistance is $R_{ac} = R_C = 3$ K

Cut-off point = $10 + 2 \times 3 = 16$ V — [Fig

Saturation point, $I_{C(sat)} = I_{CQ} + \dfrac{V_{CEQ}}{R_{ac}} = 2 + \dfrac{10}{3} = 5.13$ mA

Hence, line joining 16 V point and 5.13 mA point gives ac load line as shown in Fig. 20. As expected, this line passes through the Q-point.

Now, $I_{CQ}.\ R_{ac} = 2 \times 3 = 6$ V and $V_{CEQ} = 10$ V. Taking the smaller quantity, maximum p output signal = 6 V. Hence, peak-to-peak value = $2 \times 6 =$ **12 V.**

Example 20.13. *Find the dc and ac load lines for CE circuit shown in Fig. 20.24 (a).*

Solution. The given circuit is identical to that shown in Fig. 20.24 (*a*) except for the addit of 6 K resistor. This makes $R_{ac} = 3$ K ‖ 6 K = 2 K because collector feeds these two resistors parallel. The dc load line would remain unaffected. Change would occur only in the ac load line.

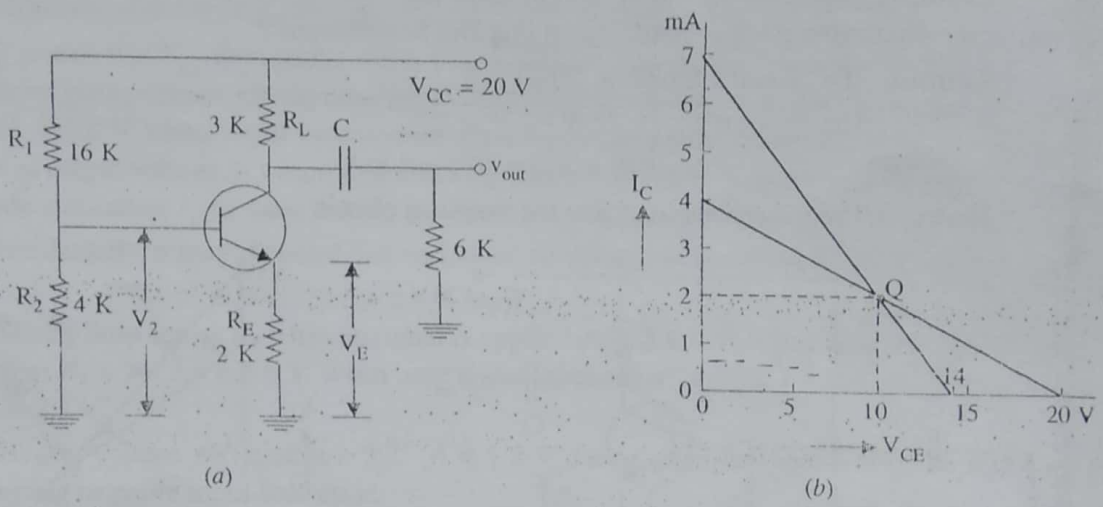

Fig. 20.25

AC Load Line

$$V_{CE(cut\text{-}off)} = V_{CEQ} + I_{CQ} R_{ac} = 10 + 2 \times 2 = \mathbf{14\ V}$$

$$I_{C(sat)} = I_{CQ} + V_{CEQ}/R_{ac} = 2 + 10/2 = \mathbf{7\ mA}$$

Example 20.14. *Draw the dc and ac load lines for the CB circuit shown in Fig. 20.26. Which swing starts clipping first ?*

Solution. The dc load line passes through cut-off point of 30 V and saturation point $V_{CC}/R_L = 1$ mA.

Now, $I_E \cong 20/40 = 0.5$ mA ; $I_C \cong I_E = 0.5$ mA; $\quad I_{CQ} = 0.5$ mA

$V_{CB} = V_{CC} - I_C R_C = 30 - 0.5 \times 30 = 15$ V ; $\quad \therefore\ V_{CBQ} = 15$ V

Hence, dc operating point or Q-point is **(15V, 0.5 mA)** as shown in Fig. 20.26 (*b*).

The cut-off point for ac load line is = $V_{CBQ} + I_{CQ} R_{ac}$.

Since collector sees an ac load of two 30 K resistors in parallel,

$\therefore \quad R_{ac} = 30$ K ‖ 30 K = 15 K.

$\therefore \quad V_{CBQ} + I_{CQ} R_{ac} = 15 + 0.5 \times 15 = 22.5$ V.

Saturation current for ac line is = $I_{CQ} + V_{CBQ}/R_{ac} = 0.5 + 15/15 = 1.5$ mA.

The line joining these two points (and also passing through Q) gives the ac load line as sh in Fig. 20.26 (*b*).

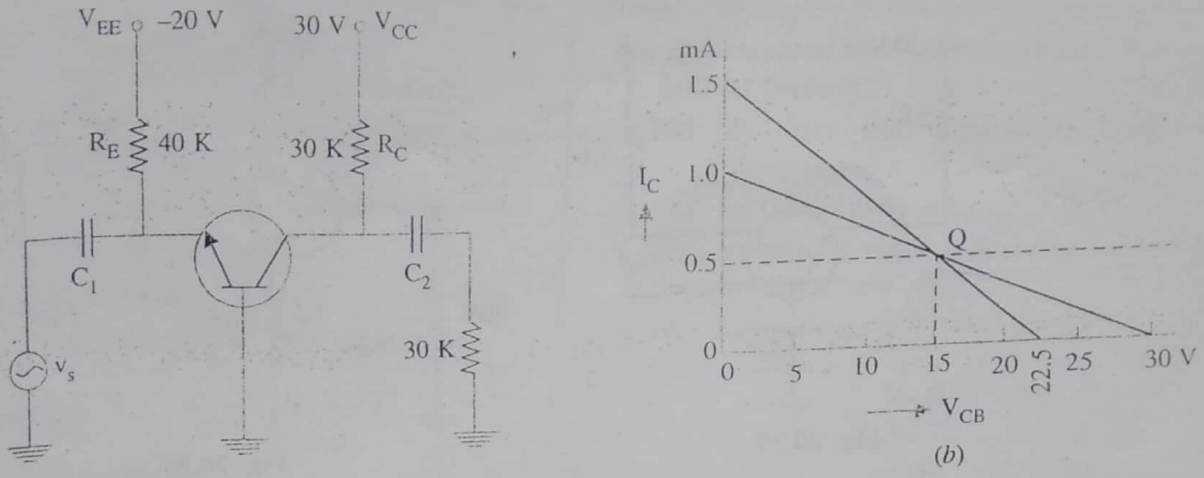

Fig. 20.26

Note. Knowing ac cut-off point and Q-point, we can draw the ac load line. Hence, we need not find the value of saturation current for this purpose.

As seen, positive swing starts clipping first because $I_{CQ}\, R_{ac}$ is less than V_{CBQ}. Obviously, maximum peak-to-peak signal that can be obtained from this circuit = 2 × 7.5 = 15 V.

Example. 20.15. *For the circuit shown in Fig. 20.26 (a), find the approximate value of source voltage v_s that will cause clipping. The voltage source has an internal resistance of 1 K.*

Solution. As found out in Ex. 20.14, the maximum swing of the unclipped output = 2 × 7.5 = 15 V.

Now,
$$A_v = \frac{v_{out}}{v_s} = \frac{R_{ac}}{R_S} = \frac{15}{1} = 15$$

$$\therefore \quad v_s = \frac{v_{out}}{A_v} = \frac{15\ V_{p-p}}{15} = 1\ V_{p-p}$$

CONVENTIONAL PROBLEMS

1. For the *CB* circuit shown in Fig. 20.27, find the approximate location of Q-point. [10 V, 2 mA]

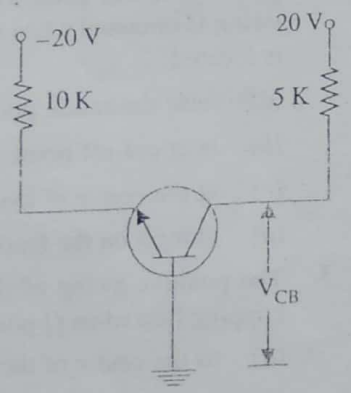

Fig. 20.27

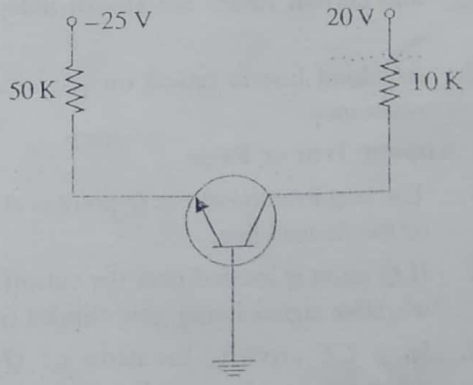

Fig. 20.28

2. For the circuit of Fig. 20.28, find
   (*a*) dc operating-point,
   (*b*) maximum peak-to-peak unclipped signal. [15 V, 0.5 mA ; 10 V_{p-p}]
3. What is the maximum peak-to-peak signal that can be obtained from the circuit of Fig. 20.29 ? [20 V_{p-p}]

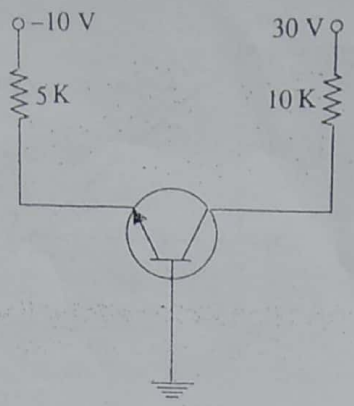

Fig. 20.29

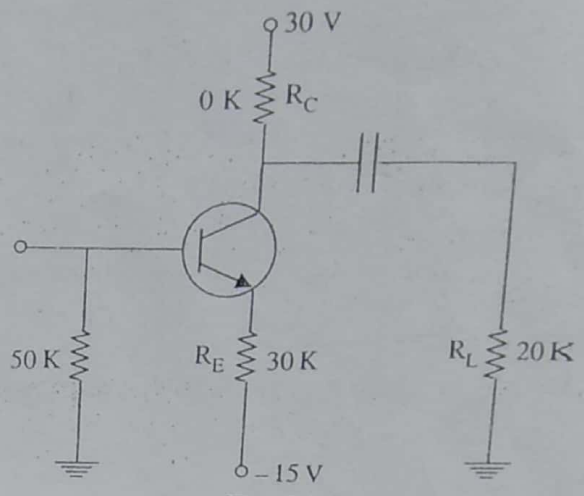

Fig. 20.30

4. Find the value of maximum peak-to-peak output of signal that can be obtained from the circuit Fig. 20.30. [10 V_{p}

SELF EXAMINATION QUESTIONS

A. Fill in the blanks with most appropriate word (s) or numerical value(s).

1. The dc load line of a transistor can be drawn if we know its cut-off and ..... points.
2. The point on the dc load line which represents value of I_C and V_{CE} that exist in the absence of input signal is called ..... point.
3. AC load line of a transistor is ..... than its dc load line.
4. A load line describes graphically the relationship between possible voltage and ..... values of a circuit.
5. An improperly-biased transistor produces ..... in the output signal.
6. In the universal bias stabilization circuit, voltage and current values are almost independent of ..... .
7. AC load line is based on ..... load resistance.

B. Answer True or False

1. The best location of the Q-point is at the centre of the dc load line.
2. If Q-point is located near the cut-off point, the negative signal swing gets clipped first.
3. In a CE circuit, location of Q-point is determined by V_{EE} and I_C.
4. The dc load line of a transistor is steeper than its ac load line.
5. In a transistor circuit, thermal stability leads to bias stability.
6. Larger the current stability factor of a circuit, greater its thermal instability.
7. Larger the β-value, greater the β-sensitiv factor of a transistor circuit.
8. β-sensitivity of a circuit depends inversely the β-value of the transistor.
9. Universal bias stabilization circuit has t highest stability factor.
10. The value of K_β varies from zero to unity.

C. Multiple Choice Items

1. The dc load line of a transistor circuit
   (*a*) has a negative slope
   (*b*) is a curved line
   (*c*) gives graphic relation between I_C and $V_{}$
   (*d*) does not contain the Q-point.
2. The maximum peak-to-peak output voltag swing is obtained when the Q-point of a circu is located.
   (*a*) near saturation point
   (*b*) near cut-off point
   (*c*) at the centre of load line
   (*d*) at least on the load line
3. The positive swing of the output signal start clipping first when Q-point of the circuit moves
   (*a*) to the centre of the load line
   (*b*) two-third way up the load line
   (*c*) towards the saturation point
   (*d*) towards the cut-off point
4. Improper biasing of a transistor circuit leads to
   (*a*) excessive heat production at collector terminal
   (*b*) distortion in output signal

(c) faulty location of load line

(d) heavy loading of emitter terminal

5. The ac load line of a transistor circuit is steeper than its dc line because

(a) ac signal sees less load resistance

(b) it has steeper slope

(c) I_C is higher

(d) input signal varies in magnitude

6. The universal bias stabilization circuit is most popular because

(a) I_C does not depend on transistor characteristics

(b) its β-sensitivity is high

(c) voltage divider is heavily loaded by transistor base

(d) I_C equals I_E

ANSWERS

A. Fill in the blanks

1. saturation 2. Q or quiescent 3. steeper 4. current 5. distortion 6. β 7. AC

B. True or False

1. *T* 2. *F* 3. *F* 4. *F* 5. *T* 6. *T* 7. *T*
8. *F* 9. *T* 10. *T*

Multiple Choice Items

1. *a* 2. *c* 3. *d* 4. *b* 5. *a* 6. *a*