***Unit 2: Flip Flop***

 **Introduction:-**

 Computers and calculators use  Flip-flop for their memory. A combination of number of flip flops will produce some amount of memory. Flip flop is formed using logic gates, which are in turn made of transistors. Flip flop are basic building blocks in the memory of electronic devices. Each flip flop can store one bit of data.

Flip – flops have two stable states and hence they are bistable multivibrators. The two stable states are High (logic 1) and Low (logic 0).

The term flip – flop is used as they can switch between the states under the influence of a control signal (clock or enable) i.e. they can ‘flip’ to one state and ‘flop’ back to other state.

* Flip – flops are a binary storage device because they can store binary data (0 or 1).
* Flip – flops are edge sensitive or edge triggered devices i.e. they are sensitive to the transition rather than the duration or width of the clock signal.
* They are also known as signal change sensitive devices which mean that the change in the level of clock signal will bring change in output of the flip flop.
* A Flip – flop works depending on clock pulses.
* Flip flops are also used to control the digital circuit’s functionality. They can change the operation of a digital circuit depending on the state.

Some of the most common flip – flops are SR Flip – flop (Set – Reset), D Flip – flop (Data or Delay), JK Flip – flop and T Flip – flop

**Types of Flip Flop:-**

Based on their operations, flip flops are basically 4 types. They are

1. R-S flip flop
2. D flip flop
3. J-K flip flop
4. T flip flop

RS Latch (1 Bit Memory Cell):-

* It is known as 1 State and 0 State. It can be obtained by using NAND or NOR gates.
* We shall be systematically developing a flip flop circuit starting from the fundamental circuit is shown below



* It consists of two inverters G1 and G2 (NAND Gates used as inverters). The output of G1 is connected to the input of G2 (B) and output of G2 is connected to the input of G1 (A).
* Let us assume the output of G1 to be Q=1, which is also the input of G2(B=1) therefore the output of G2 will be $\overbar{Q}=0$, which makes A=0 and consequently which confirms our assumption.
* In a similar manner, it can be demonstrated that if Q=0 then $\overbar{Q}=1$ and this is also consistent with the circuit connection.
* **From the above discussion we know the following**
1. Output $Q and\overbar{Q}$ are always complementary
2. This circuit has to stable state: in one of the state Q=0, which is referred to as the zero state.
3. If the circuit is in 1 state it continues to remain in this state and similarly, if it is in 0 state it continues to remain in this state this property of the circuit is referred as memory.

i.e. it can store 1-Bit of digital information.

**Key Points**

The 2 outputs are always complementary.

The circuit has 2 stable states. When Q=1, it is **Set state**. When Q=0, it is **Reset state**.

The circuit can store 1-bit of digital information and so it is called one-bit memory cell.

The one-bit information stored in the circuit is locked or latched in the circuit. This circuit is also called **Latch**

**SR Flip-Flop:-**

Flip-flops and latches are used as data storage elements. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics.



**Working:-**

**Case 1:**

When both the SET and RESET inputs are low, then the output remains in previous state i.e. it holds the previous data.

**Case 2:**

When SET input is high and RESET input is low, then the flip flop will be in SET state. Because Set input is high(1) the output of G3 will be low and the output goes to input of G1 gate and also Reset input is low(0) the output of G4 will be High and when one of the input of G1 is zero the output will be 1 and the output of G2 will be 0, means SET state.

**Case 3:**

When SET input is low and RESET input is high, then the flip flop will be in RESET state. Because Set input is Low (0) the output of G3 will be 1 and Reset input is high (1) the output of G4 will be 0. This will cause the output of the flip – flop to settle in RESET state.

**Case 4:**

When both the SET and RESET inputs are high, then the flip flop will be undefined state. Because the high inputs of S and R, violates the rule of flip flop that the outputs should complement to each other. So the flip flop is in undefined state (or forbidden state).

**Clocked SR Flip Flop:-**

It is often required to set or reset the memory cell in synchronism with a train of pulses known as clock. Such a circuit is shown below and is referred to as a clocked set-reset (S-R) Flip Flop.In this circuit if a clock pulse is present (Clk =1), its operation is exactly the same as SR flip-flop.

On the other hand, when the clock pulse is not present (Clk= 0), the gate G3 and G4 are inhibited. That is there output are 1 irrespective of the values of S or R.

In other words the circuit responds to the inputs S and R only when the clock is present.

When the clock pulse is present the truth table of clocked SR flip flop same as that of SR flip flop

****

The circuit of clocked SR flip – flop using NAND gates is shown above.



**Application**

SR flip – flops are very simple but are not widely used in practical circuits because of their illegal state where both S and R are high (S = R = 1). But they are used in switching circuits as they provide simple switching function (between Set and Reset). One such application is a Switch de – bounce circuit. The SR flip – flops are used to eliminate mechanical bounce of switches in digital circuits.

**Clocked SR flip flop with preset and clear:-**

In the flip flop when the power is switched on the state of the circuit is uncertain it may come to set (Q=1) or reset (Q=0) state.

In many applications it is desired to initially set or reset the flip flop. i.e. the initial state of the flip flop is to be assigned. This is accomplished by using preset and clear inputs.

These inputs may be applied at any time between clocks pulses are not in synchronism with the clock. An S R flip flop with preset and clear is shown in figure



If Pr=Cr=1 the circuit operates in accordance with the truth table of S-R Flip Flop

If Pr=0 and Cr=1, the output of G1 (Q) will certainly be 1.

Consequently all the three inputs to G2 will be 1 which will make$\overbar{Q}=0$. Hence making Pr=0 sets the flip flop. 

Similarly if Pr=1 and Cr=0 then the flip flop is reset.

The condition Pr=Cr=0 must not be used, since this leads to an uncertain state.

**J-K Flip Flop:-**

JK flip – flop is named after Jack Kilby, the electrical engineer who invented IC. A JK flip – flop is called a Universal Programmable flip – flop because, using its inputs J, K Preset and Clear, function of any other flip – flop can be imitated.

A JK flip – flop is the modification of SR flip – flop with no illegal state. In this the J input is similar to the SET input of SR flip – flop and the K input is similar to the RESET input of SR flip – flop. The symbol of JK flip – flop is shown below.



JK flip – flop logic diagram is shown in the figure. As said before, JK flip – flop is a modified version of SR flip – flop. Logic diagram consists of three input NAND gates replacing the two inputs NAND gates in SR flip – flop and the inputs are replaced with J and K from S and R.

The design of the JK flip-flop is such that the three inputs to one NAND gate are J, clock signal along with a feedback signal from Q’ and the three inputs to the other NAND are K, clock signal along with a feedback signal from Q. This arrangement eliminates the indeterminate state in SR flip-flop.



Operation

##### Case 1: When both the inputs J and K are LOW, then Q returns its previous state value i.e. it holds the previous data.

When we apply a clock pulse to the J K flip flop and the J input is low then irrespective of the other NAND gates, the NAND G3 output becomes HIGH. In the same manner, if the K input is low then output of NAND G4 is also HIGH. So thus the output remains in the same state i.e. no change in the state of flip flop.

##### Case 2: When J is LOW and K is HIGH, then flip flop will be in Reset state i.e. Q = 0, $\overbar{Q}$ = 1.

When we apply a clock pulse to the J K flip flop and the inputs are J is low and K is high the output of the NAND gate connected to J input becomes 1. Then Q becomes 0. This will reset the flip flop again to its previous state. So the Flip flop will be in RESET state.

##### Case 3: When J is HIGH and K is LOW, then flip – flop will be in Set state i.e. Q = 1, $\overbar{Q}$ = 0

When we apply a clock pulse to the J K flip flop and the inputs are J is high and K is low the output of the NAND gate connected to K input becomes 1. Then $\overbar{Q}$ becomes 0. This will set the flip flop with the high clock input. So the Flip flop will be in SET state.

##### Case 4: When both the inputs J and K are HIGH, then flip – flop is in Toggle state. This means that the output will complement of the previous state.

**Race around condition of JK Flip Flop:-**

 Race around condition occurs in a JK Flip Flop when the Inputs are:

J = 1 and K = 1.

As we know, there’s a concept called as Toggling. If you don’t know, know it. The output signals of Q and $\overbar{Q}$ keep on changing like:

Q: 0 1 0 1 0 … and

$\overbar{Q}$: 1 0 1 0 ….

Now, Toggling means the same as above. But, the Toggling occurs when the delay time is equal to the clock pulse. So, there’s just a single change in the signal. If the initial state is 0, toggling it would make it 1 and vice versa. So, just one change in one toggle.

While, in case of Racing, the delay is greater than the clock pulse. So, there’s very fast changing of the output signal in a single clock pulse without any change in the Input.

The Race around condition isn’t in control. So, it needs to be bought in control. There are 3 ways to do so:

1] Increase the clock pulse.

2] Edge Triggering

3] Master Slave

**Master Slave J K Flip Flop:-**

* The master slave JK flip flop is a combination of a clocked JK latch and a clocked SR latch. The clocked JK latch acts as the master and the clocked SR latch acts as the slave.
* Master is positive level triggered and due to the presence of an inverter in the clock line, the slave is negative level edge triggered. Hence when clock=1, the master is active and slave is inactive. Vice versa happens when clock=0.



The following is truth table of master slave flip flop.



**Operation:-**

**Case I:** When clock is not given, both master and slave are inactive and there will be no change in outputs.

**Case II:** For clock=1, master is active, slave inactive. As J=K=0, output of master i.e. Q and $\overbar{Q}$ will not change. As soon as clock goes to 0, slave becomes active, and master inactive. But since input to slave S and R is same, output of slave will also remain same.

**Case III:** For clock=1, master is active and slave is inactive. When J=0 and K=1, outputs of master will be Q=0, $\overbar{Q}$=1, which will be inputs to slave. When clock=0, slave becomes active and takes inputs 0, 1 to give output Q=0, $\overbar{Q}$=1. This output will not change if clock is again made 1and then 0. Hence we get a stable output from master and slave.

**Case IV:** For clock=1, master is active and slave is inactive. When J=1 and K=0, outputs of master will be Q=1, $\overbar{Q}$=0, which will be inputs to slave. When clock=0, slave becomes active and takes inputs 1, 0 to give output Q=1, $\overbar{Q}$=0. This output will not change if clock is again made 1 and then 0. Hence we get a stable output from master and slave.

**Case V:** When clock =1, J=K=1, master output will toggle. So S and R will invert. But slave remains inactive all this time since clock is 1. As soon as clock becomes 0, slave becomes active and master becomes inactive. So slave will also toggle. These changed outputs are returned through feedback to the master, but master does not respond to them because clock is now 0 and master is inactive. Thus, in one clock period, master and slave both toggles only once, avoiding race condition caused by multiple toggling.

**D Flip Flop:-**

D flip – flops are also called as “Delay flip – flop” or “Data flip – flop”. They are used to store 1 – bit binary data. They are one of the widely used flip – flops in digital electronics. Apart from being the basic memory element in digital systems, D flips – flops are also considered as Delay line elements and Zero – Order Hold elements.

D flip – flop has two inputs, a clock (CLK) input and a data (D) input and two outputs; one is main output represented by Q and the other is complement of Q represented by$ \overbar{Q}$. The symbol of a D flip – flop is shown below.



**Construction:-**

A D flip – flop is constructed by modifying an SR flip – flop. The S input is given with D input and the R input is given with inverted D input. Hence a D flip – flop is similar to SR flip – flop in which the two inputs are complement to each other, so there will be no chance of any intermediate state occurs. The major drawback of SR flip – flop is the race around condition which in D flip – flop is eliminated (because of the inverted inputs). The circuit diagram of D flip – flop is shown in below figure.

**Working**

When we don’t apply any clock input to the D flip flop or during the falling edge of the clock signal, there will be no change in the output. It will retain its previous value at the output Q. If the clock signal is high (rising edge to be more precise) and if D input is high, then the output is also high and if  D input is low, then the output will become low. Hence the output Q follows the input D in the presence of clock signal.



Simply, for positive transition on clock signal,

If D = 0 => Q = 0 so flip flop is reset.

If D = 1 => Q = 1 so flip flop is set.

NOTE: **↑** indicate positive edge of the clock and ↓ indicate negative edge of the clock signal.



**Positive edge triggered D Flip Flop with clock Pulse**

**Applications-**

D flip – flops are one of the most widely used flip – flops. Some of the many applications of D flip – flop are

* Data storage registers.
* Data transferring as shift registers.
* Frequency division circuits.

**T Flip-Flop:-**

 T flip-flop is also known as “Toggle Flip-flop”. To avoid the occurrence of intermediate state in SR flip-flop, we should provide only one input to the flip – flop called Trigger input or Toggle input (T). Then the flip-flop acts as a Toggle switch. Toggling means ‘Changing the next state output to complement of the present state output’. We can design the T flip – flop by making simple modifications to the JK flip-flop. The T flip-flop is a single input device and hence by connecting J and K inputs together and giving them with single input called T we can convert a JK flip-flop into T flip-flop. So a T flip-flop is sometimes called as single input JK flip-flop.

The logic symbol of T flip-flop is shown below with the truth table. 

It has one Toggle input (T) & one clock signal input (CLK)

The simplest of the constructions of a D flip – flop is with JK flip – flop. The J input and K input of the JK flip – flop are connected together and provided with the T input. The logic circuit of a T flip – flop constructed from a JK flip – flop is shown below.

T flip-flop is an edge triggered device i.e. the low to high or high to low transitions on a clock signal of narrow triggers that is provided as input will cause the change in output state of flip-flop.



In simple terms, the operation of the T flip – flop is

When the T input is low, then the next sate of the T flip flop is same as the present state.

* T = 0 and present state = 0 then the next state = 0
* T = 1 and present state = 1 then the next state = 1

When the T input is high and during the positive transition of the clock signal, the next state of the T flip – flop is the inverse of present state.

* T = 1 and present state = 0 then the next state = 1
* T = 1 and present state = 1 then the next state = 0

As each incoming trigger alternately changes the set and reset inputs, the flip – flop toggles. So to complete one full cycle of output wave form it need two triggers. This means that the T flip flop produces the output at exactly half of the frequency of input frequency. So a T flip – flops will act as “Frequency Divider Circuit”.

The main disadvantage of T flip – flop is that the state of the flip – flop at an applied trigger pulse is known only when the previous state is known.