UNIT – I

8085 MICROPROCESSOR

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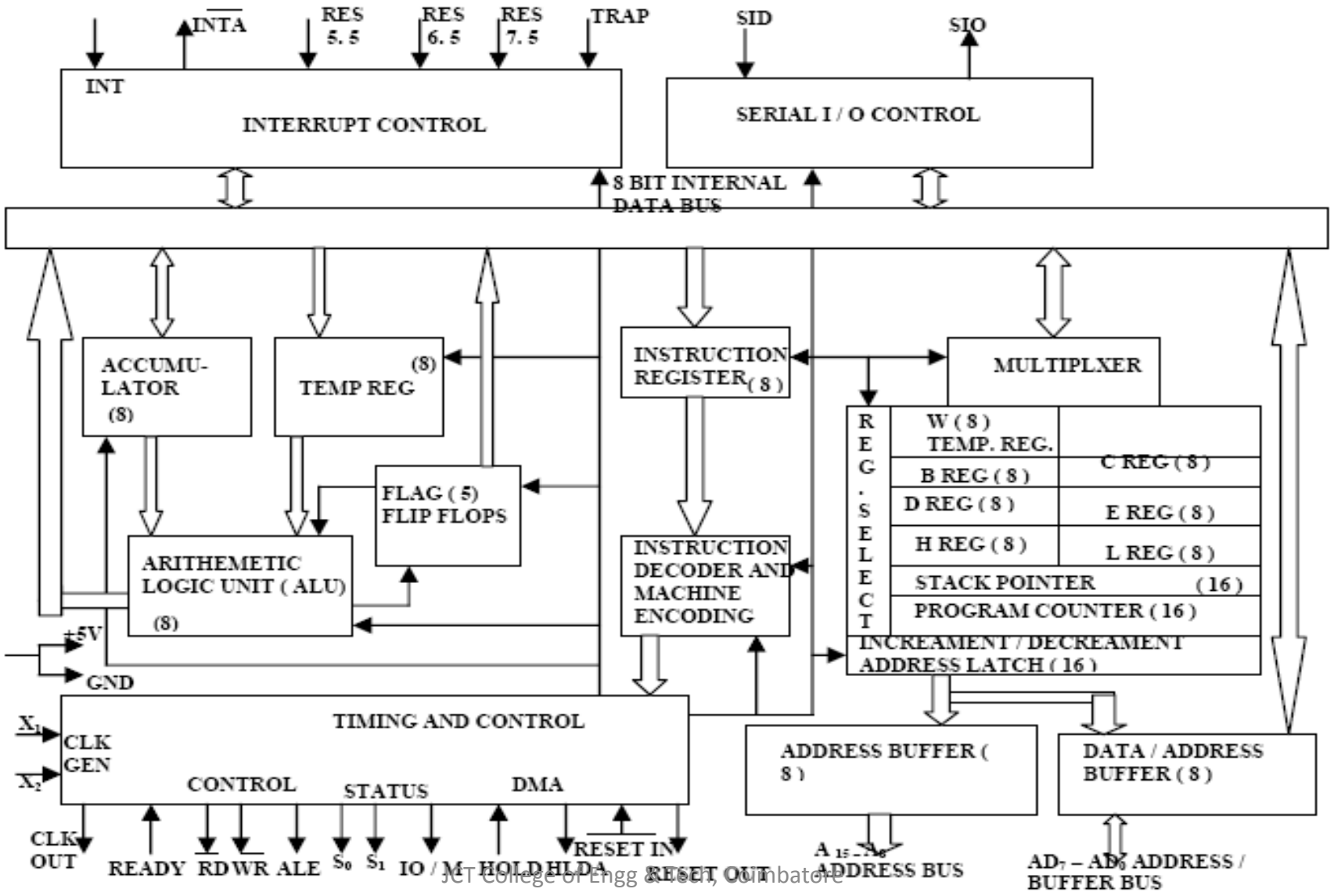
CHAPTERS

- Hardware Architecture
- Pin outs
- Functional Building Blocks of Processor
- Memory organization
- I/O ports
- Data transfer concepts
- Timing Diagram
- Interrupts.

HARDWARE ARCHITECTURE



CPU INTERNAL STRUCTURE

Registers

- Six general purpose 8-bit registers: B, C, D, E, H, L.
- They can also be combined as register pairs to Perform 16-bit operations: BC, DE, HL.
- Registers are programmable (data load, move, etc.)
- Accumulator Single 8-bit register that is part of the ALU !
- Used for arithmetic / logic operations – the result is always stored in the accumulator.

Program Counter (PC)

- This is a register that is used to control the sequencing of the execution of instructions.
- This register always holds the address of the next instruction.
- Since it holds an address, it must be 16 bits wide.

Stack Pointer (SP)

- The stack pointer is also a 16-bit register that is used to point into memory.
- The memory this register points to is a special area called the stack.
- The stack is an area of memory used to hold data that will be retreived soon.
- The stack is usually accessed in a Last In First Out (LIFO) fashion.

ARITHMETIC AND LOGIC UNIT

- In addition to the arithmetic & logic circuits, the ALU includes the accumulator, which is part of every arithmetic & logic operation.

- Also, the ALU includes a temporary register used for holding data temporarily during the execution of the operation. This temporary register is not accessible by the programmer.

ACCUMULATOR

- A register in which intermediate arithmetic and logic results are stored.
- Example for accumulator use is summing a list of numbers.
  - ✓ The accumulator is initially set to zero, then each number in turn is added to the value in the accumulator.
  - ✓ Only when all numbers have been added is the result held in the accumulator written to main memory or to another, non-accumulator, CPU register.

DATA BUS

- The data bus is 'bi-directional'
  - ✓ data or instruction codes from memory or Input/output are transferred into the microprocessor
  - ✓ the result of an operation or computation is sent out from the microprocessor to the memory or input/output.

- Depending on the particular microprocessor, the data bus can handle 8 bit or 16 bit data.

ADDRESS BUS

- The address bus is '**unidirectional**', over which the microprocessor sends an address code to the memory or input/output.
- The size (width) of the address bus is specified by the number of bits it can handle.
- The more bits there are in the address bus, the more memory locations a microprocessor can access.
- A 16 bit address bus is capable of addressing 65,536 (64K) addresses.

CONTROL BUS

- The control bus is used by the microprocessor to send out or receive timing and control signals in order to coordinate and regulate its operation and to communicate with other devices, i.e. memory or input/output.

THE CONTROL AND STATUS SIGNALS

- There are 4 main control and status signals. These are:
  - ✓ **ALE:** Address Latch Enable. This signal is a pulse that become 1 when the AD0 – AD7 lines have an address on them. It becomes 0 after that. This signal can be used to enable a latch to save the address bits from the AD lines.
  - ✓ **RD:** Read. Active low.
  - ✓ **WR:** Write. Active low.
  - ✓ **IO/M:** This signal specifies whether the operation is a memory operation (IO/M=0) or an I/O operation (IO/M=1).
  - ✓ **S1 and S0 :** Status signals to specify the kind of operation being performed .Usually un-used in small systems.

FREQUENCY CONTROL SIGNALS

- There are 3 important pins in the frequency control group.
  - ✓ X0 and X1 are the inputs from the crystal or clock generating circuit.
  - ✓ The frequency is internally divided by 2.
    - ❖ So, to run the microprocessor at 3 MHz, a clock running at 6 MHz should be connected to the X0 and X1 pins.
  - ✓ CLK (OUT): An output clock pin to drive the clock of the rest of the system.

FLAG REGISTER

It is an 8-bit register, in which five of the bits carry significant information in the form of flags : S (Sign flag), Z (Zero flag), AC (Auxiliary carry flag), P (Parity flag), and CY (carry flag), as shown in Fig. 2.2.

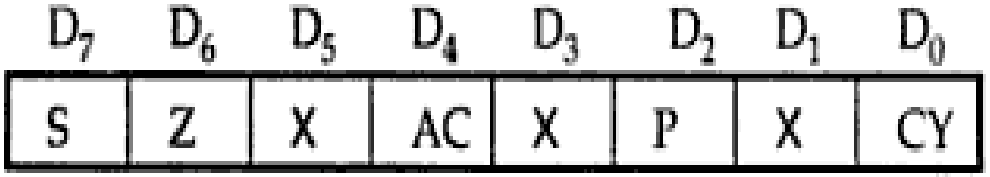


Fig. 2.2 Flag register

S-Sign flag : After the execution of arithmetic or logical operations, if bit D_7 of the result is 1, the sign flag is set. In a given byte if D_7 is 1, the number will be viewed as negative number. If D_7 is 0, the number will be considered as positive number.

Z-Zero flag : The zero flag sets if the result of operation in ALU is zero and flag resets if result is non zero. The zero flag is also set if a certain register content becomes zero following an increment or decrement operation of that register.

AC-Auxiliary Carry flag : This flag is set if there is an overflow out of bit 3 i.e. , carry from lower nibble to higher nibble (D_3 bit to D_4 bit). This flag is used for BCD operations and it is not available for the programmer.

P-Parity flag : Parity is defined by the number of ones present in the accumulator. After an arithmetic or logical operation if the result has an even number of ones, i.e. even parity, the flag is set. If the parity is odd, flag is reset.

CY-Carry flag : This flag is set if there is an overflow out of bit 7. The carry flag also serves as a borrow flag for subtraction. In both the examples shown below, the carry flag is set.

PIN DESCRIPTION

- 8085 is a 40 pin IC, The signals from the pins can be grouped as follows
- 1. Power supply and clock signals
  2. Address bus
  3. Data bus
  4. Control and status signals
  5. Interrupts and externally initiated signals
  6. Serial I/O ports

POWER SUPPLY AND CLOCK FREQUENCY SIGNALS

- **Vcc:** + 5 volt power supply
- **Vss:** Ground.
- **X1, X2 :** Crystal or R/C network or LC network connections to set the frequency of internal clock generator. The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected externally. CLK (output)-Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

ADDRESS BUS

- A8 - A15: (output; 3-state) It carries the most significant 8 bits of the memory address or the 8 bits of the I/O address.

DATA BUS

- AD0 - AD7 (input/output; 3-state) These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.
- During the op code fetch operation, in the first clock cycle, the lines deliver the lower order address A0 - A7.
- In the subsequent IO / memory, read / write clock cycle the lines are used as data bus.
- The CPU may read or write out data through these lines.

CONTROL AND STATUS SIGNALS

ALE (output) - Address Latch Enable.

- It is an output signal used to give information of AD0-AD7 contents.
- It is a positive going pulse generated when a new operation is started by uP.
- When pulse goes high it indicates that AD0-AD7 are address.
- When it is low it indicates that the contents are data.

RD (output 3-state, active low)

- Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device

WR (Write)

- Write memory or IO device.
- This indicates that the data on the data bus is to be written into the selected memory location or I/O device.

IO/M (output) - Select memory or an IO device

- This status signal indicates that the read / write operation relates to whether the memory or I/O device.
- It goes high to indicate an I/O operation.
- It goes low for memory operations.

STATUS SIGNALS

`S1:` `S2:`

It is used to know the type of current operation of the microprocessor.

IO/M	S1	S0	OPERATION
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	0	Interrupt acknowledge
Z	0	1	Halt
Z	x	x	Hold
Z	x	x	Reset

INTERRUPTS AND EXTERNALLY INITIATED OPERATIONS

- They are the signals initiated by an external device to request the microprocessor to do a particular task or work.
- There are five hardware interrupts called,

  TRAP

  RST 7.5

  RST 6.5

  RST 5.5

  INTA
- On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.

Reset In (Input)

- This signal is used to reset the microprocessor.
- The program counter inside the microprocessor is set to zero.
- The buses are tri-stated.

Reset Out (Output)

- It indicates CPU is being reset.
- Used to reset all the connected devices when the microprocessor is reset.

DIRECT MEMORY ACCESS (DMA)

- When 2 or more devices are connected to a common bus, to prevent the devices from interfering with each other, the tri state gates are used to disconnect all devices except the one that is communicating at a given instant.
- The CPU controls the data transfer operation between memory and I/O device. Direct Memory Access operation is used for large volume data transfer between memory and an I/O device directly.
- The CPU is disabled by tri-stating its buses and the transfer is effected directly by external control circuits.

- **HOLD signal** is generated by the DMA controller circuit. On receipt of this signal, the microprocessor acknowledges the request by sending out

- **HLDA signal** and leaves out the control of the buses. After the HLDA signal the DMA controller starts the direct transfer of data.

READY (input)

- Memory and I/O devices will have slower response compared to microprocessors.
- Before completing the present job such a slow peripheral may not be able to handle further data or control signal from CPU.
- The processor sets the READY signal after completing the present job to access the data.
- The microprocessor enters into WAIT state while the READY pin is disabled.

SINGLE BIT SERIAL I/O PORTS

- SID (input) Serial input data line
- SOD (output) Serial output data line
- These signals are used for serial communication.