UNIT-II NOTES

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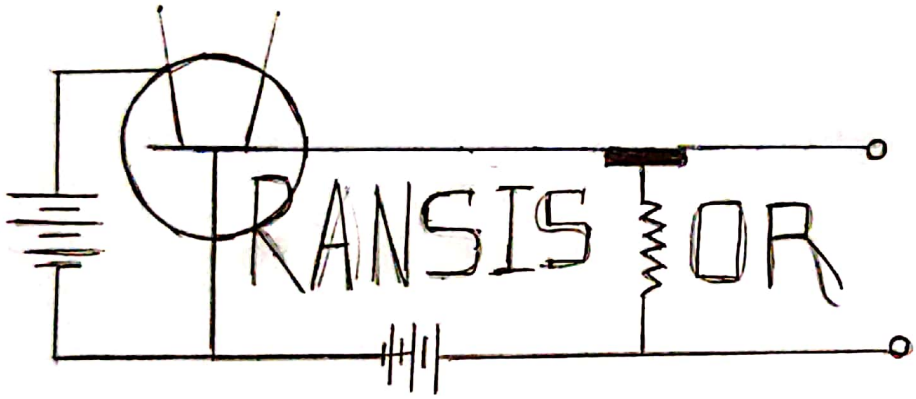
B.Sc FIRST YEAR

SEMESTER - II

ELECTRONICS



* ## TRANSISTOR :-

A Transistor consists of two pn junctions formed by "sandwiching either p-type or n-type semiconductor between a pair of opposite types.

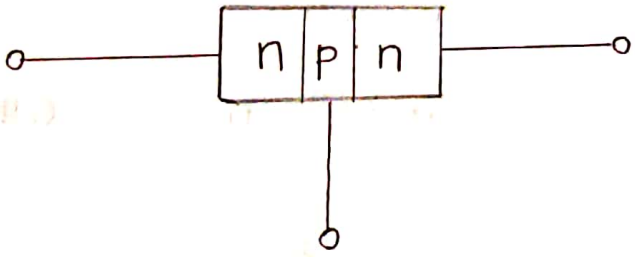
There are 2 types of Transistors :-

i) n-p-n Transistor

ii) p-n-p Transistor

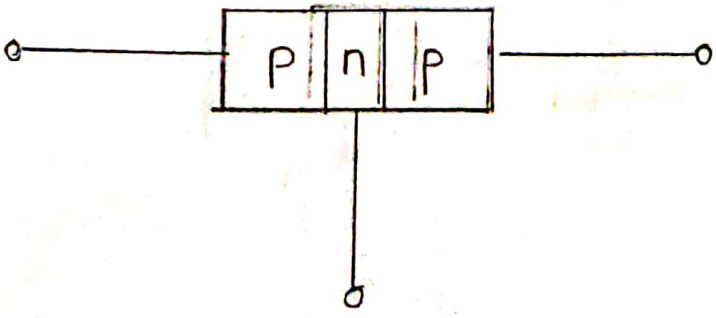
i) n-p-n Transistor :-

An n-p-n transistor is composed of two n-type semiconductors seperated by a thin section of p-type as shown in fig.



ii) P-n-P Transistor :-

A P-n-P Transistor is formed by two P-sections seperated by thin section of n-type as shown in fig.



In each type of transistor, the following points may be noted

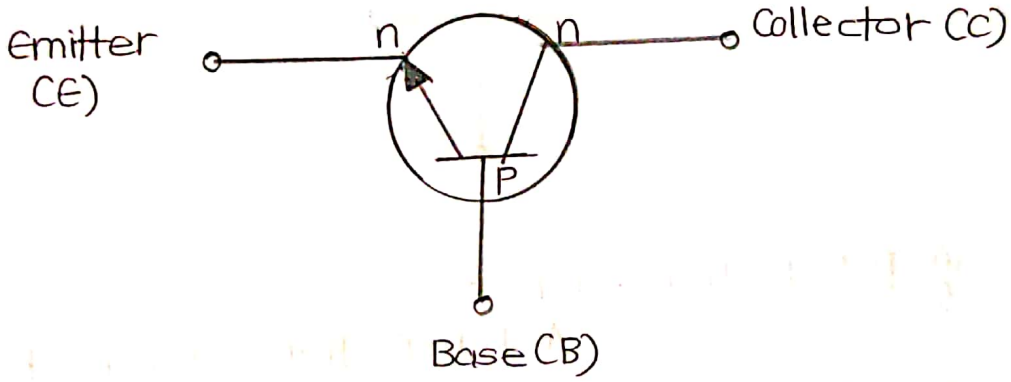
i) These are two pn junctions. Therefore, a transistor may be regarded as a combination of two diodes connected back to back.

ii) There are three terminals, one taken from each type of semiconductor.

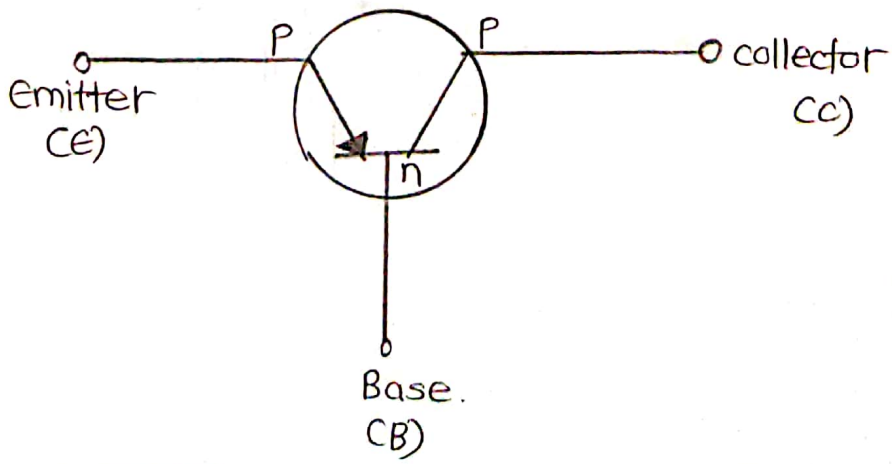
iii) The Middle section is a very thin layer. This is the most important factor in the function of a transistor.

* SYMBOLS :-

i) n-p-n Transistor :-



ii) P-n-p Transistor :-



* ## Construction of Transistor :-

A Transistor (pnp or npn) has 3 sections of doped semiconductors. The section on one side is the emitter and the section the opposite is the collector. The Middle section is called as the Base and forms two junctions between the emitter and collector.

i) Emitter :-

The section on one side that supplies charge carriers (electrones or holes) is called the Emitter. The emitter is always forward biased w.r.t base. so that it can supply a large no. of majority carriers.

In fig i) the emitter (p-type) of pnp transistor is forward biased & supplies hole charges to its junction with the base.

Similarly in fig ii) the emitter (n-type) of npn transistor has a forward bias and supplies free electrones to its junction with the base.

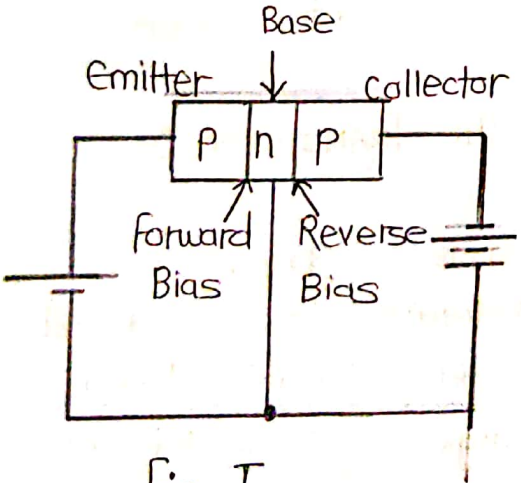


Fig. I

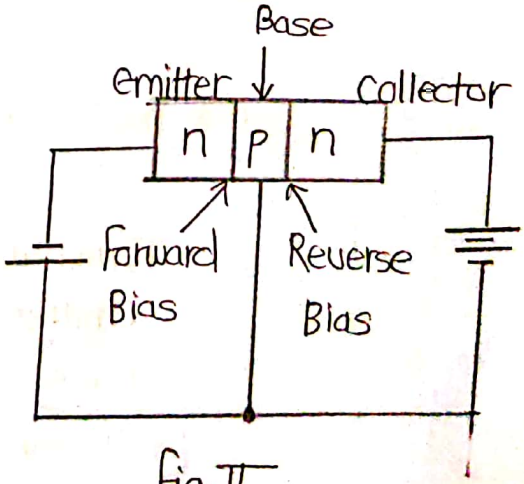


Fig. II

II) Collector :-

The section on the other side that collects the charges is called the collector. The collector is always reverse biased. It's function is to remove charges from its junction with the Base.

In fig I,

The collector (P-Type) of pnp transistor has a reverse bias and receives holes charges that flow in the output circuit.

Similarly, in fig II,

The collector of npn transistor has reverse bias and receives electrones.

III) Base :-

The Middle Section which forms two pn junctions between the emitter and collector is called the base. The base-emitter junction is forward biased, allowing low resistance for the emitter ckt. The base-collector junction is reverse biased & provides high resistance in the collector circuit.

Some Facts About The TRANSISTOR :-

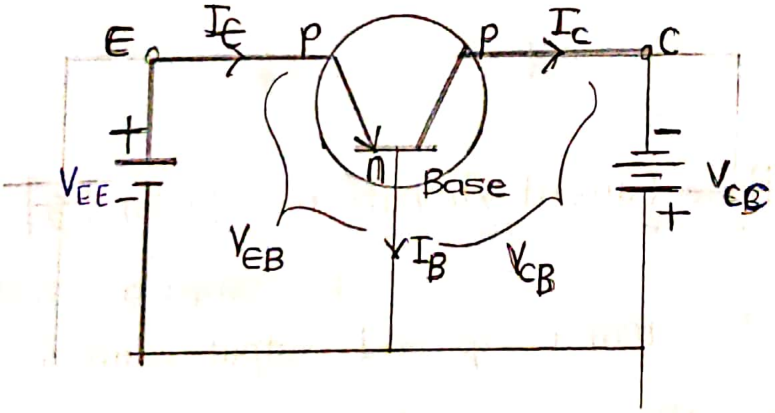
Terminals	Size	Doping
Emitter	Moderate	strongly doped
Base	small	Lightly doped
Collector	Large	Moderately doped

TRANSISTOR Connections :-

There are three leads in a transistor i.e. emitter, base and collector terminals.
A Transistor can be connected in a circuit in the following three ways.

A] Common Base Configuration :-

In this arrangement, input is applied between emitter and base & output is taken from collector & base. Here, base of the transistor is common to both input and output circuits and hence the name common base connection.



* Current Amplification Factor [α] :-

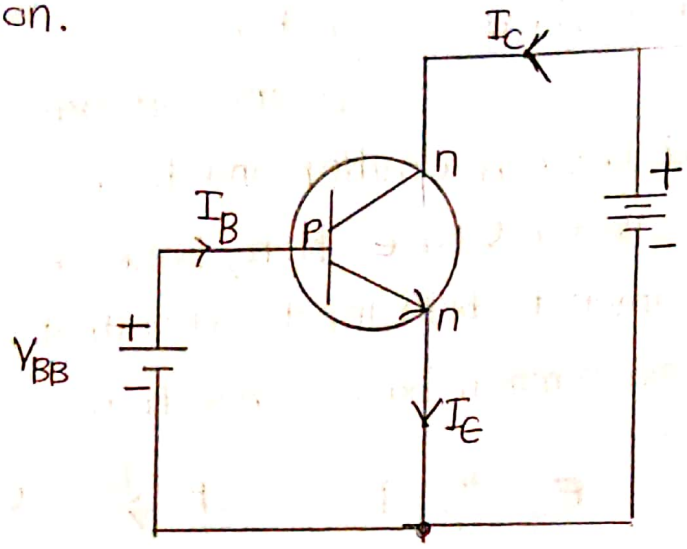
It is the ratio of output current to input current. In a common base connection, the input current is the emitter current I_E & output current is the collector current I_C.

$$\therefore \alpha = \frac{\text{output current}}{\text{Input current}}$$

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

B] Common Emitter Connection :-

In this arrangement, input is applied between base and emitter and output is taken from the collector and Emitter. Here, Emitter of the transistor is common to both input and output circuits and hence the name common emitter connection.



* Base Current Amplification Factor [β] :-

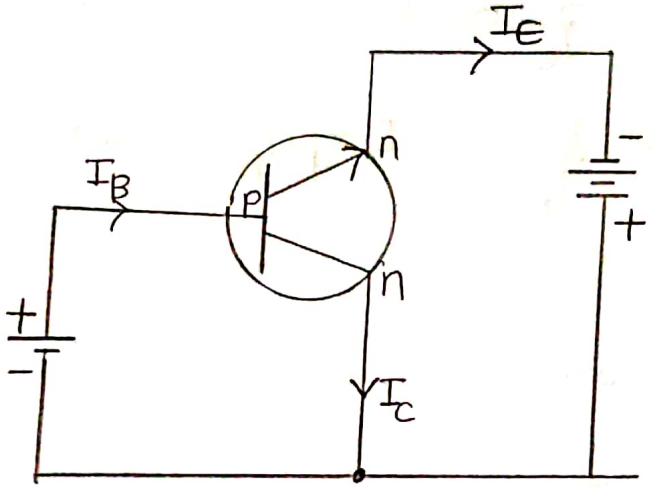
In common emitter connection, input current is 'I_B' and output current is 'I_C'. The ratio of output current 'I_C' to the Input Current 'I_B'.

$$\therefore \beta = \frac{\text{output Current}}{\text{Input Current}}$$

$$\boxed{\beta = \frac{I_C}{I_B}}$$

C] Common Collector Connection :-

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector. Here, collector of the transistor is common to both input & output circuits & hence the name common collector connection.



* Current Amplification Factor :- [γ]

It is a ratio of output current i.e 'I_E' to the input current 'I_B'.

$$\therefore \gamma = \frac{I_E}{I_B}$$

* Relation Between $\alpha, \beta, \& \gamma$:-

Emitter Current = Base Current + Collector Current

$$I_E = I_B + I_C \quad \text{——— (I)}$$

As, we know that

$$\alpha = \frac{I_C}{I_E} \Longrightarrow I_C = \alpha \cdot I_E \quad \text{——— (II)}$$

$$\beta = \frac{I_C}{I_B} \Longrightarrow I_C = \beta \cdot I_B \quad \text{——— (III)}$$

Now,

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_C + I_B} \quad \text{---- from eqn (I) } [\text{i.e } I_E = I_C + I_B]$$

$$\alpha = \frac{\beta \cdot I_B}{\beta \cdot I_B + I_B} \quad \text{--- from eqn (III)}$$

$$\alpha = \frac{\beta I_B}{(\beta + 1) I_B}$$

$$\boxed{\alpha = \frac{\beta}{(1 + \beta)}}$$

Now, $\beta = \frac{I_C}{I_B}$

$$\beta = \frac{I_C}{I_E - I_C}$$

$$\left[\begin{array}{l} I_E = I_C + I_B \\ \text{since} \\ I_B = I_E - I_C \end{array} \right]$$

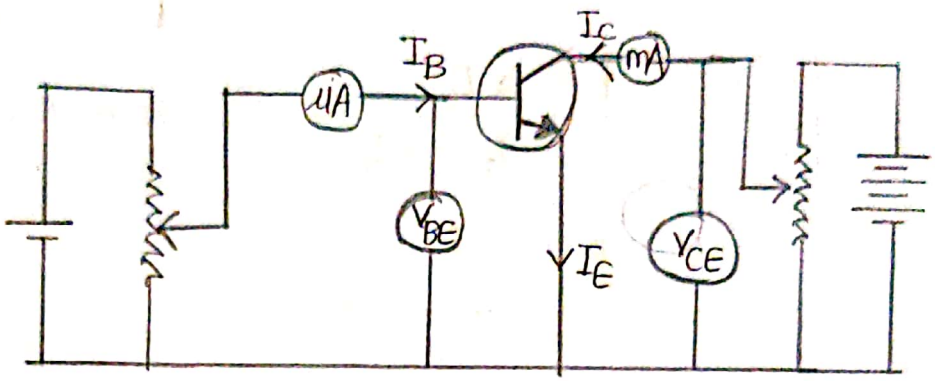
$$\beta = \frac{\alpha I_E}{I_E - \alpha I_E} \quad \text{--- from eqn (11)}$$

$$\beta = \frac{\alpha I_E}{I_E (1 - \alpha)}$$

$$\boxed{\beta = \frac{\alpha}{(1 - \alpha)}}$$

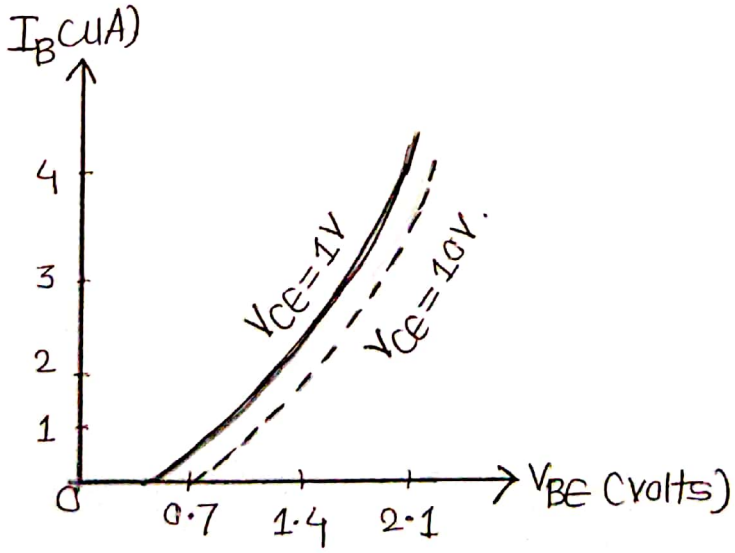
* Characteristics of COMMON EMITTER CONNECTION :-

The important characteristics of this circuit arrangement are the input characteristics & output characteristics.



I] Input Characteristics OR Base Curve :-

It is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.



The Input Characteristics of a CE connection can be determined by the circuit as shown in figure. keeping V_{CE} = constant (say at 10V), note the base current 'I_B' for various values of V_{BE}. Then plot the readings obtained on the graph, taking I_B along Y-axis & V_{BE} along x-axis. This gives the input characteristics at V_{CE} = 10V as shown in fig. following a similar procedure, a family of input characteristics can be drawn. The following points may be noted from the Characteristics.

i) The characteristics resembles that of a forward biased diode curve. This is expected that since the base-emitter section of transistor is a diode & it is forward biased.

ii) As compared to CB arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a CE circuit is higher than that of CB circuit.

iii) Input Resistance :- It is a ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} i.e

$$\text{Input Resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

The value of r_i for a CE circuit is of the order of a few hundread Ohms.

II] Output Characteristics or Collector Curve :-

It is the curve between collector current 'I_C' and collector- emitter voltage V_{CE} at constant base current I_B.

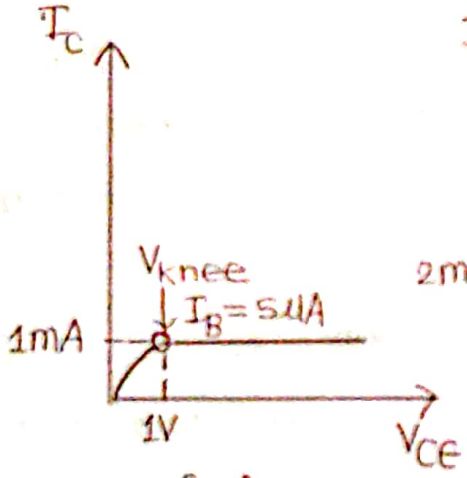


fig i

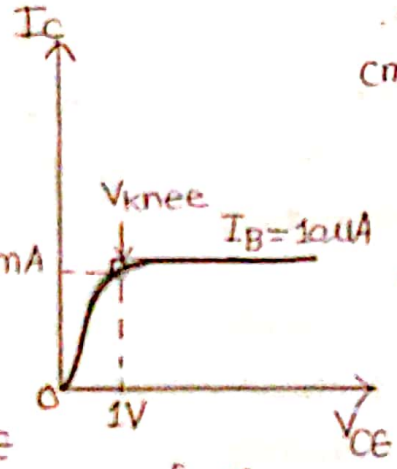


fig ii

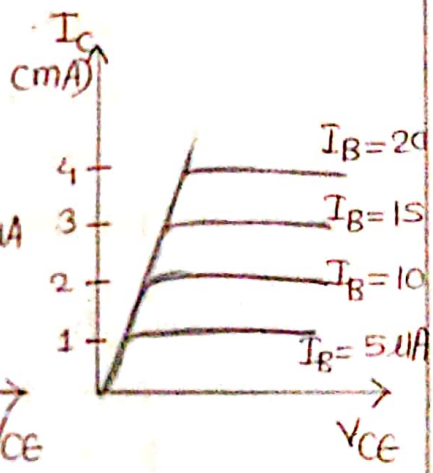


fig iii

The output characteristics of a CE circuit can be drawn with the help of the circuit as shown in above figures.

~~The output characteristics of a CE circuit can be drawn with the help of the~~ Keeping the base current I_B fixed at some value say 5uA, note the collector current I_C for various values of V_{CE}. Then plot the readings on a graph, taking I_C along y-axis & V_{CE} along x-axis.

This gives the output characteristics at $I_B = 5uA$ as shown in fig. i. The test can be repeated for $I_B = 10uA$ to obtain the new output characteristics as shown in fig. ii. following similar procedure, a family of output characteristics can be drawn as shown in fig. iii.

The following points may be noted from the characteristics:

i) The collector current I_C varies with V_{CE} between 0 and 1V only. After this, collector current becomes almost constant and independent of V_{CE}. This value of V_{CE} upto which collector current I_C changes with V_{CE} is called the knee voltage. The transistor are always operated in the region above knee voltage.

ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carries before electron -hole combinations occur in the base area.

iii) for any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

Output Resistance :- It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B i.e

$$\text{output Resistance} :- r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B.$$

It may be noted that whereas the output characteristics of CB circuit are horizontal, they have noticeable slope for the CE circuit. Therefore, the output resistance of a CE circuit is less than that of CB circuit. Its value is of the order of 50 kΩ.

* Operation of Bipolar Junction Transistor [BJT] in Active, cut-off, Saturation & Inverted Active Mode ?

→ BJT has two junctions Base-Emitter Junction [J_{BE}] and Base-Collector Junction [J_{BC}].
Accordingly, there are 4 regions of operation in which either of two junctions are forward biased or reverse biased or both.

A] F-R Bias :-

When Base-Emitter junction is forward biased and Base-collector junction is reverse biased The Transistor operates in Active Region.
In this region the current flowing through the npn transistor are

a) Emitter Current :- 'I_E'

A forward current flows from Emitter into Base consisting of electrones and hole current flowing from Base to Emitter.

b) Base Current :- 'I_B'

As the electrones enters into the base region the recombination takes place & recombination current flows from the base which is exactly equal to the rate at which holes are lost in Base. The current will be small as base is lightly doped & no. of charge carriers are less.

Also a reverse saturation current flows from Base to collector as the Base-Collector is reverse biased.

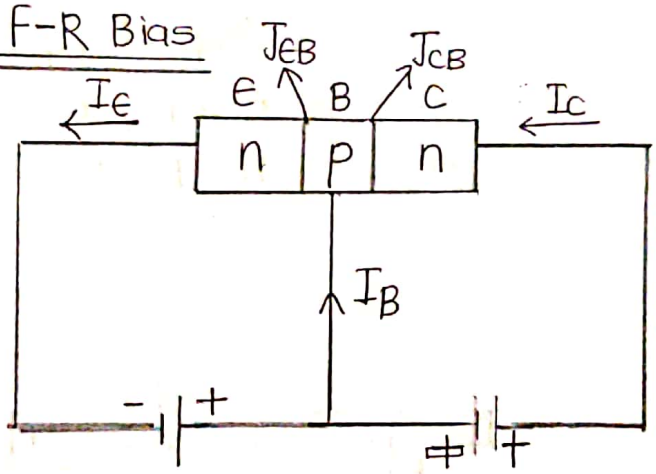
c) Collector Current :- 'Ic'

As collector is moderately doped In case of npn transistor the collector has moderate no of electrones.

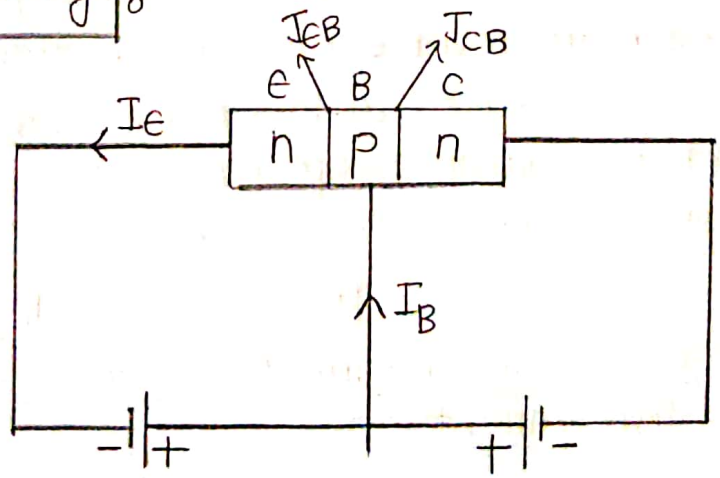
As some electrones will recombine with the holes in the base region & remaining electrones will cross Base-Collector junction & try to flow through the collector region.

From the collector end to the +ve end of battery & constitute a collector current 'Ic'.

Diagram :- F-R Bias



B] F-F Biasing



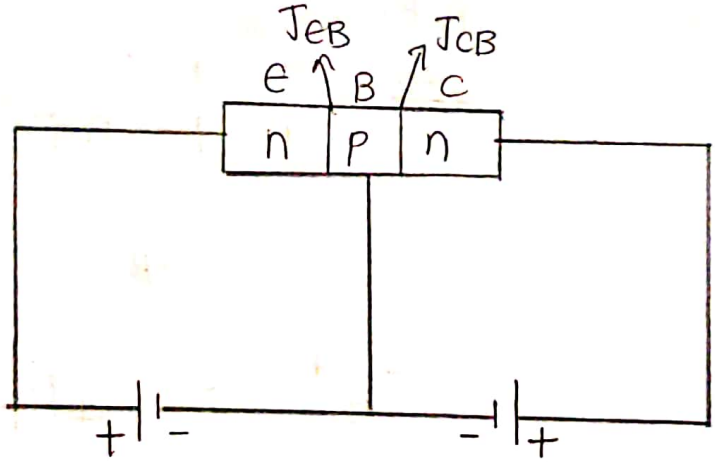
When both J_{EB} & J_{BC} Junctions of the transistor are forward biased the transistor operates in saturation region.

- P.T.O

Continue:- In this region high current flows through the transistor as both the junction of transistor are forward biased & resistance offered is much less. This is due to the fact that along with electron current flowing from Emitter to Base in active region. There will be addition of electron current flowing from collector to Base.

In F-F Biasing Transistor acts as a Closed Switch.

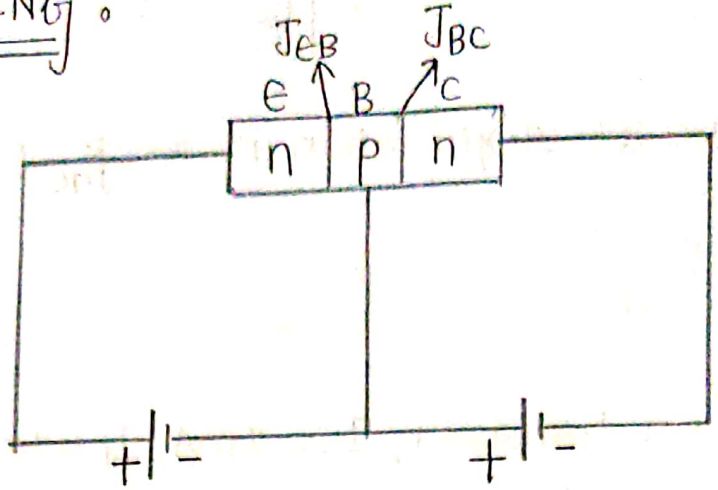
c] R-R Biasing :-



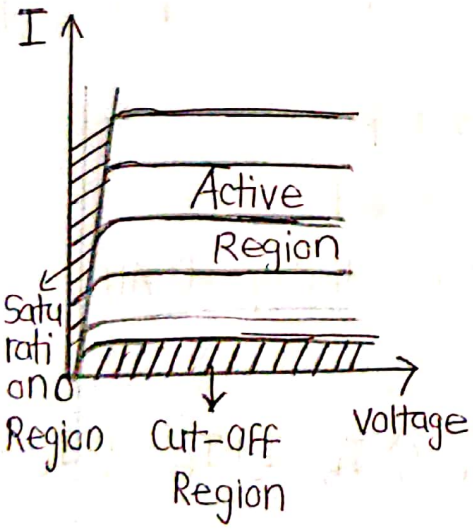
When both the junction of the transistor are reverse biased the transistor operates in cut-off region. In this region transistor does not conduct any current except for reverse saturation current that flows across the junction.

In Cut-off Condition Emitter current is zero & collector current consist of small reverse saturation current.

D] R-F BIASING :-



When J_{EB} is Reverse Biased & J_{BC} junction is forward biased the transistor works in Inverted Active Region. When you interchange the roles off both the junctions, the conventional current flows from Emitter to Collector but this is not ideal case of Transistor. Hence, the Inverted Active Mode is not preferable.



J_{EB}	J_{BC}	Region	Uses
F	R	Active Region	Amplifier
F	F	Saturation Region	closed switch
R	R	cut-off	open switch
R	F	Inverted Active Region	Less Amplification.

Q. 5 Marks Question ?

I) Describe Collector Curve for CE Transistor with necessary diagram ?

II) Explain in detail [F-R] bias applied to NPN Transistor ?

III) Explain CE Characteristics of Transistor ?

IV) Give the Construction with proper symbols of PNP & NPN Transistor ?

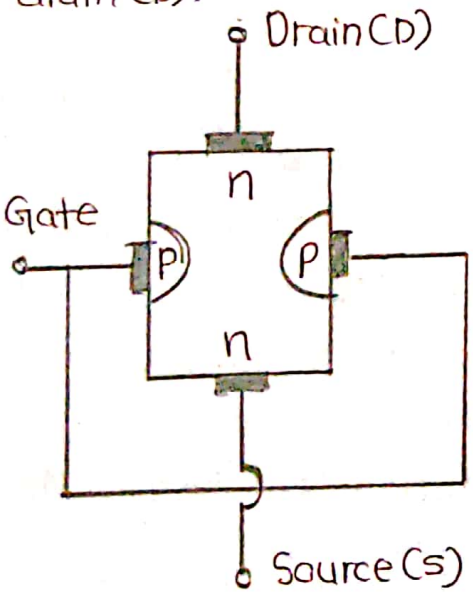
*

Junction Field Effect Transistor [JFET] :-

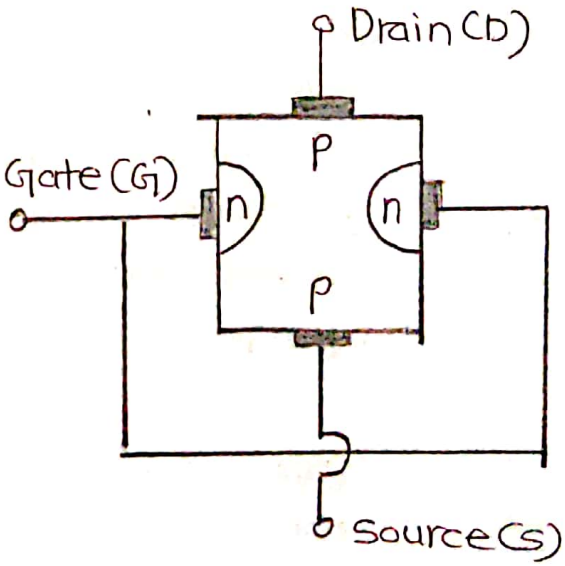
A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e electrones or holes.

Construction :-

A JFET consists of a P-Type or n-Type silicon bar containing two pn junctions at the sides as shown in fig. The bar forms the conducting channel for the charge carriers. If the bar is of n-type it is called n-channel JFET. And if the bar is of P-Type, it is called a P-channel JFET. The two pn junctions forming diodes are connected internally and a common terminal called Gate is taken out. Other terminals are source and Drain taken out from the bar. Thus a JFET has essentially three terminals viz, gate (G), source (S), drain (D).



n-Channel JFET



P-Channel JFET.

Principle & Working of JFET :-

Principle :- The two pn junctions at the sides form two depletion layers. The current conduction by charge carriers (i.e free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease.

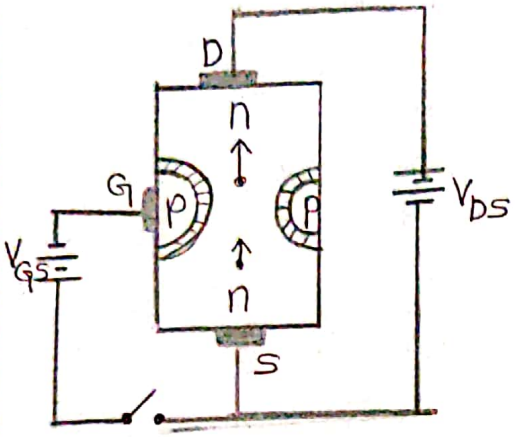
Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.

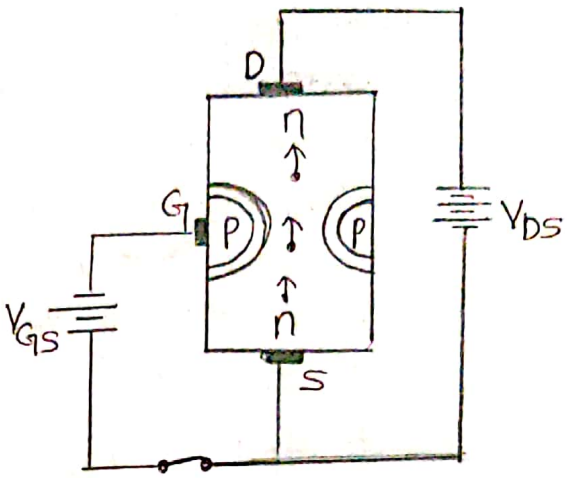
Working :-

i) When a voltage V_{DS} is applied between drain & source terminals & voltage on the gate is zero, the two pn junctions at the sides of the bar establish depletion layers. The electrones will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

ii) When a reverse voltage V_{GS} is applied between the gate and source, the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased. on the other hand, if the reverse voltage on the gate is decreased, the width of depletion layer also decreases

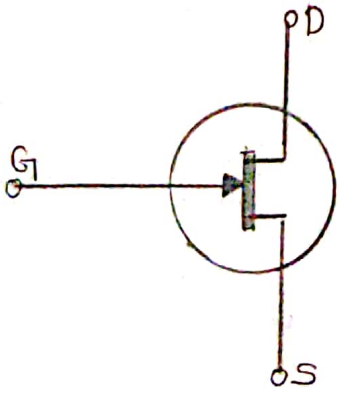
This increases the width of the conducting channel and hence source to drain current.



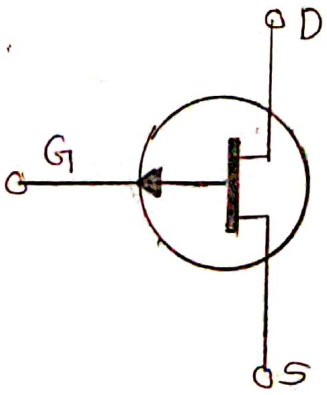


It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e electric field) on the gate. For this reason, the device is called Field Effect Transistor. It may be noted that a p-channel JFET operates in the same manner as n-channel JFET except that channel current carriers will be holes instead of electrones & the polarities of V_{GS} & V_{DS} are reversed.

* SYMBOLS :-



n-channel JFET

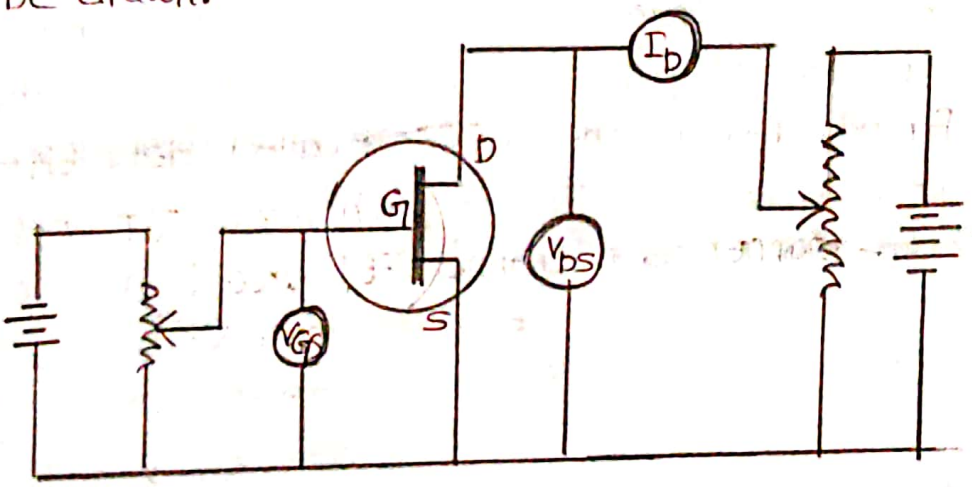


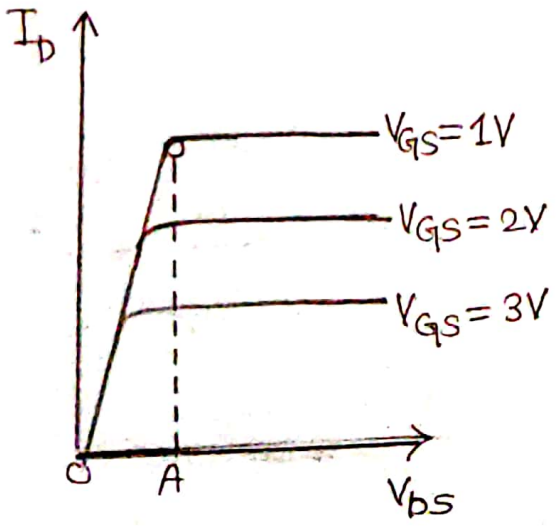
P-Channel JFET.

* Output Characteristics of JFET :-

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate-source voltage (V_{GS}) is known as output characteristics of JFET.

Keeping V_{GS} fixed at some value, say 1V, the drain-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristics of JFET at $V_{GS} = 1V$. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn.





The following points may be noted from the Characteristics:-

i) At first, the drain current I_D rises rapidly with drain - source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as Pinch Off Voltage. V_p.

ii) After pinch-off Voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. ∴ Increase in drain current is very small with V_{DS} above pinch-off Voltage. Consequently, drain current remains constant.

* METAL OXIDE SEMICONDUCTOR FET (MOSFET) :-

The main drawback of JFET is that its gate must be reversed biased for proper operation of the device i.e it can only have negative gate operation for n-channel and positive gate operation for p-channel.

This means that we can only decrease the width of the channel (i.e decrease the conductivity of the channel) from its zero-bias size. This type of operation is referred to as depletion mode operation. ∴ a JFET can only be operated in the depletion mode.

However, there is a field effect transistor that can be operated to enhance (or increase) the width of the channel (with consquent increase in conductivity of the channel) i.e it can have enhancement mode operation. Such a FET is called MOSFET.

A field effect transistor [FET] that can be operated in the enhancement-mode is called a MOSFET.

* Types of MOSFETs :-

There are 2 basic types of MOSFET :-

A] Deplection Type MOSFET or D-MOSFET :-

The D-MOSFET can be operated in both the depletion-mode & enhancement mode.

B] Enhancement-Type MOSFET OR E-MOSFET :-

The E-MOSFET can be operated only in enhancement mode.

A] D-MOSFET :-

Construction :-

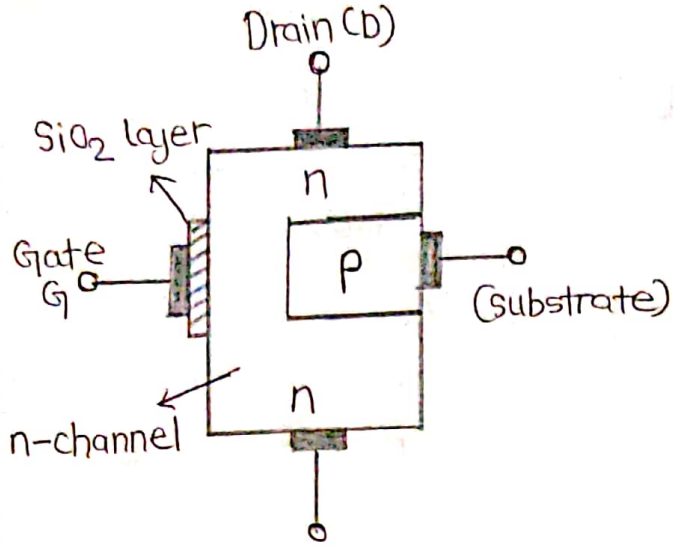
i) The n-channel D-MOSFET is a piece of n-type material with a p-type channel (called substrate) on the right and an insulated gate on the left. The free electrones flowing source to drain must pass through the narrow channel between the gate and the p-type region.

ii) A thin layer of metal oxide (usually SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric.

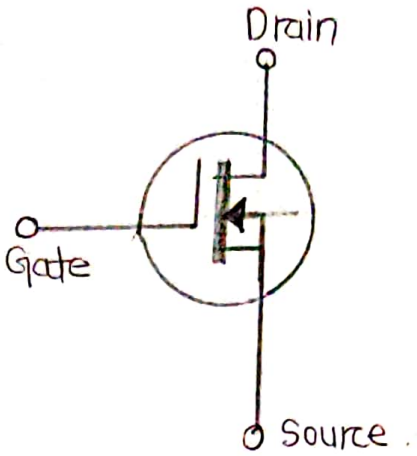
iii) It is a usual practise to connect the substrate to the source (S) internally so that a MOSFET has three terminals viz Source (S), gate (G) & drain (D).

iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. ∴

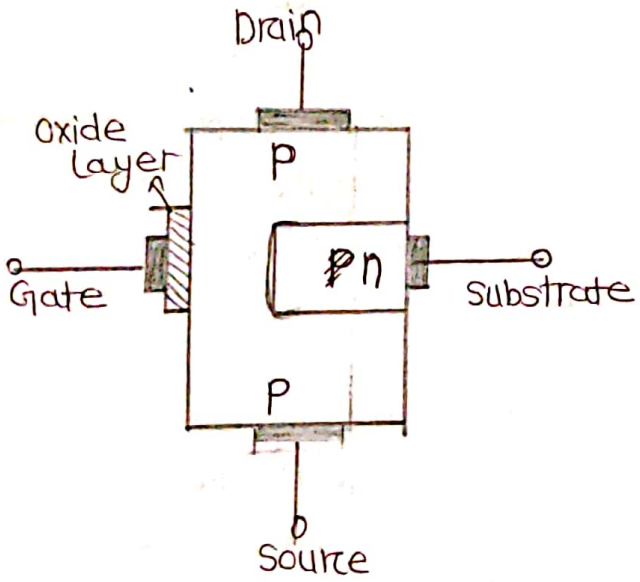
Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode. However, JFET can be operated only in depletion Mode.



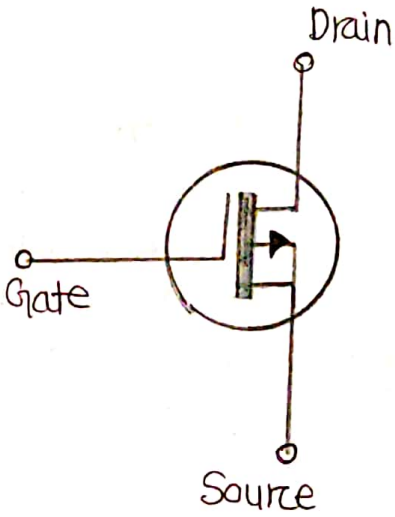
n-Channel D-MOSFET



n-channel D-MOSFET.

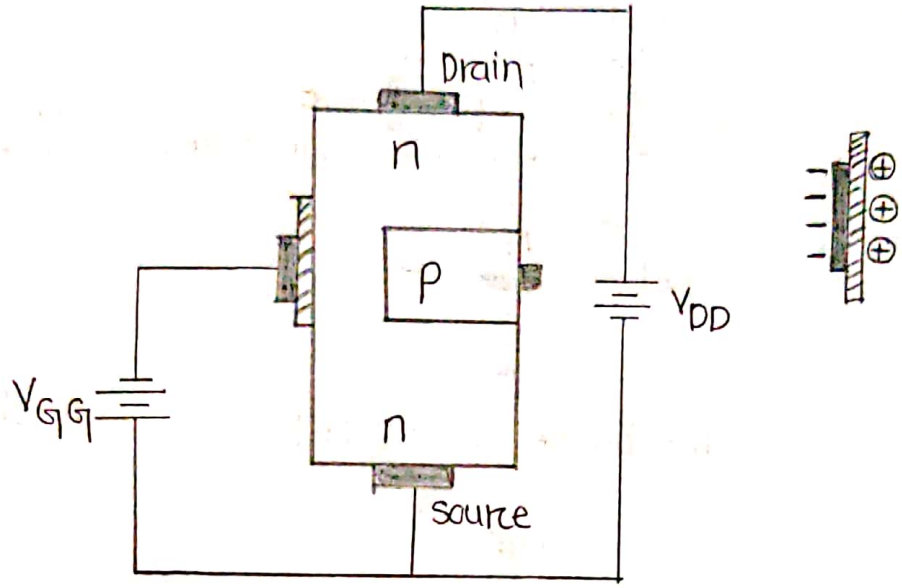


P-channel D-MOSFET



* Operation of D-MOSFET :-

a) Depletion Mode :-

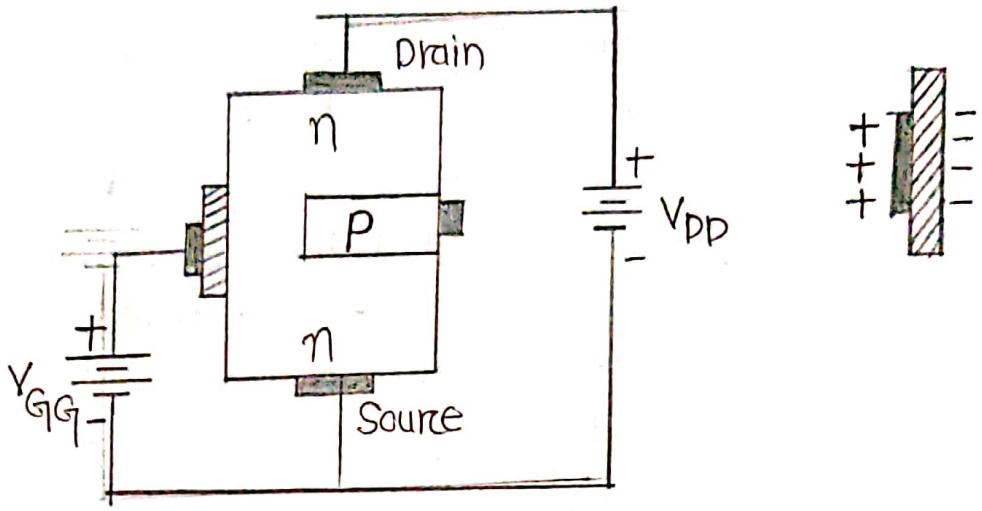


i) Fig. shows depletion mode operation of n-channel D-MOSFET. Since gate is negative, it means electrones are on the gate.

ii) These electrones repel the free electrones in the n-channel, leaving a layer of positive ions in a part of the channel as shown in fig. In other words, we have depleted (i.e emptied) the n-channel of some of its free electrones. Therefore, lesser number of free electrones are made available for current conduction through the n-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel & hence the current from source to drain. Note that with -ve voltage to the gate, the action of D-MOSFET is similar to JFET. Because the action with negative gate depends upon depleting the channel of free electrones, the negative-gate operation is called depletion Mode.

b) Enhancement Mode :-



Above figure shows enhancement mode operation of n-channel D-MOSFET. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the n-channel as shown in fig. These negative charges are the free electrones drawn into the channel. Because these free electrones are added to these already in the channel, the total number of free electrones in the channel is increased. Thus a positive gate voltage enhances or increases the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between D-MOSFET and JFET is that we can apply positive gate voltage to D-MOSFET and still have essentially zero current. Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.

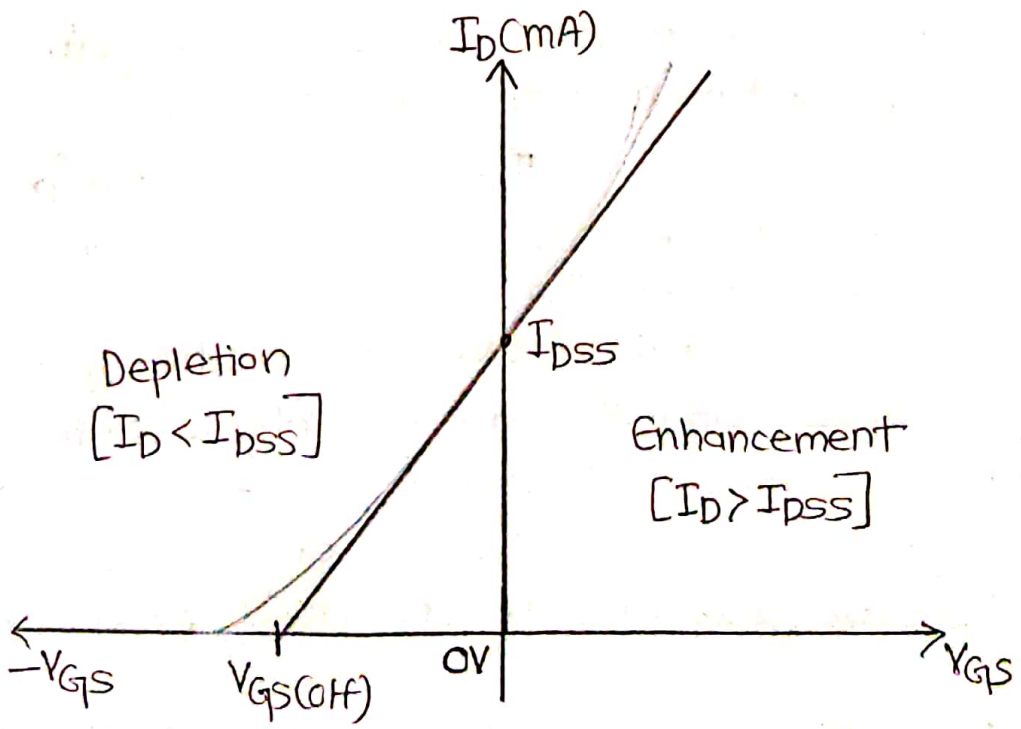
The following points may be noted about D-MOSFET operation.

i) In a D-MOSFET, the source to drain current is controlled by the electric field of capacitor formed at the gate.

ii) The gate of JFET behaves as a reverse biased diode whereas the gate of a D-MOSFET acts like a capacitor. for this reason, it is possible to operate D-MOSFET with positive or negative gate voltage.

iii) As the gate of D-MOSFET forms a capacitor, therefore negligible gate current flows whether positive or negative voltage is applied to the gate. for this reason, the input impedence of D-MOSFET is very high ranging from 10,000 MΩ to 10,000,00 MΩ.

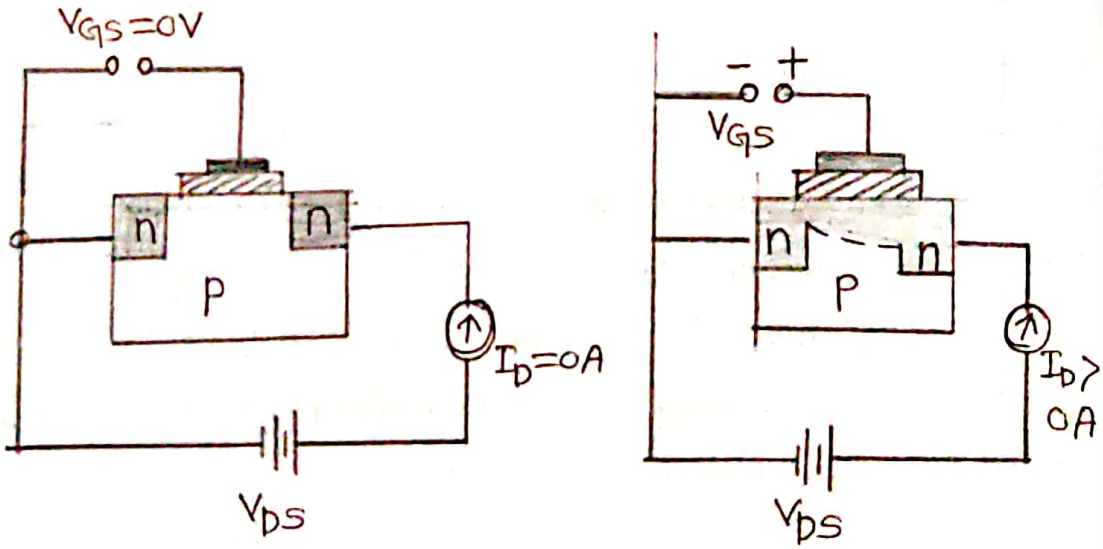
* D-MOSFET Transfer Characteristic :-



* Enhancement Type MOSFET :-

Two things are worth nothing about E-MOSFET. First, E-MOSFET operates only in the Enhancement mode and has no depletion mode. Secondly, the E-MOSFET has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer. It is only by the application of V_{GS} (gate to source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the E-MOSFET is called Threshold voltage [$V_{GS(th)}$]. The n-channel device requires positive V_{GS} [$\geq V_{GS(th)}$] & the p-channel device requires negative V_{GS} [$\geq V_{GS(th)}$].

* Operation of E-MOSFET :-



n-channel E-MOSFET.

P.T.O

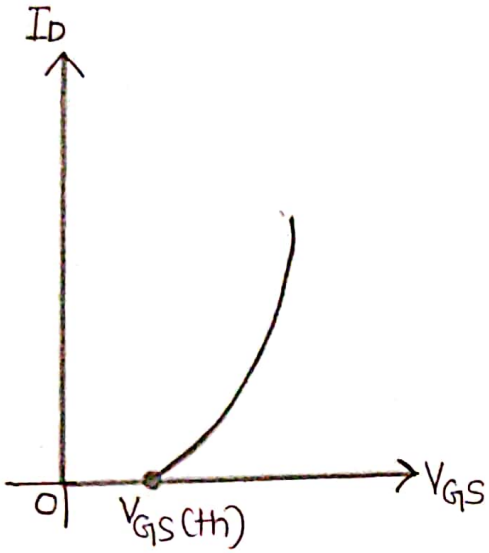
Working :-

i) When $V_{GS}=0V$, there is no channel connecting the source and drain. The P substrate has only a few thermally produced free electrones (minority carriers) so that drain current is essentially zero. for this reason, E-MOSFET is normally off when $V_{GS}=0V$.

ii) When gate is made positive (i.e V_{GS} is positive) as shown in fig. it attracts free electrones into the p-region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain.

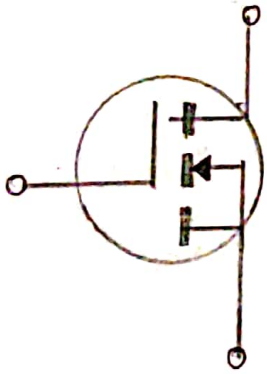
"The minimum value of V_{GS} that turns the E-MOSFET ON is called threshold voltage [$V_{GS(th)}$].

iii) When V_{GS} is less than $V_{GS(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS(th)}$, the E-MOSFET is turned ON and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS(th)}$, if the value of V_{GS} ~~decreases~~ is increased, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS(th)}$]. the channel becomes ~~wider~~ narrower and I_D will decrease. This fact is revealed by the transconductance curve of n-channel E-MOSFET shown in fig. As you can see, $I_D=0$, when $V_{GS}=0$. Therefore the value of I_{DSS} for the E-MOSFET is zero. Also that there is no drain current until V_{GS} reaches $V_{GS(th)}$.

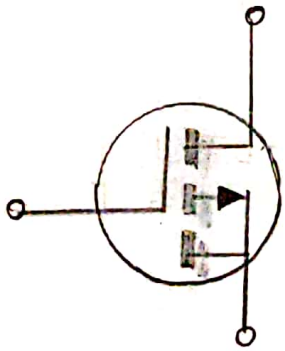


n-channel

* Symbols :-



n-Channel E-MOFSET



P-channel E-MOSFET.