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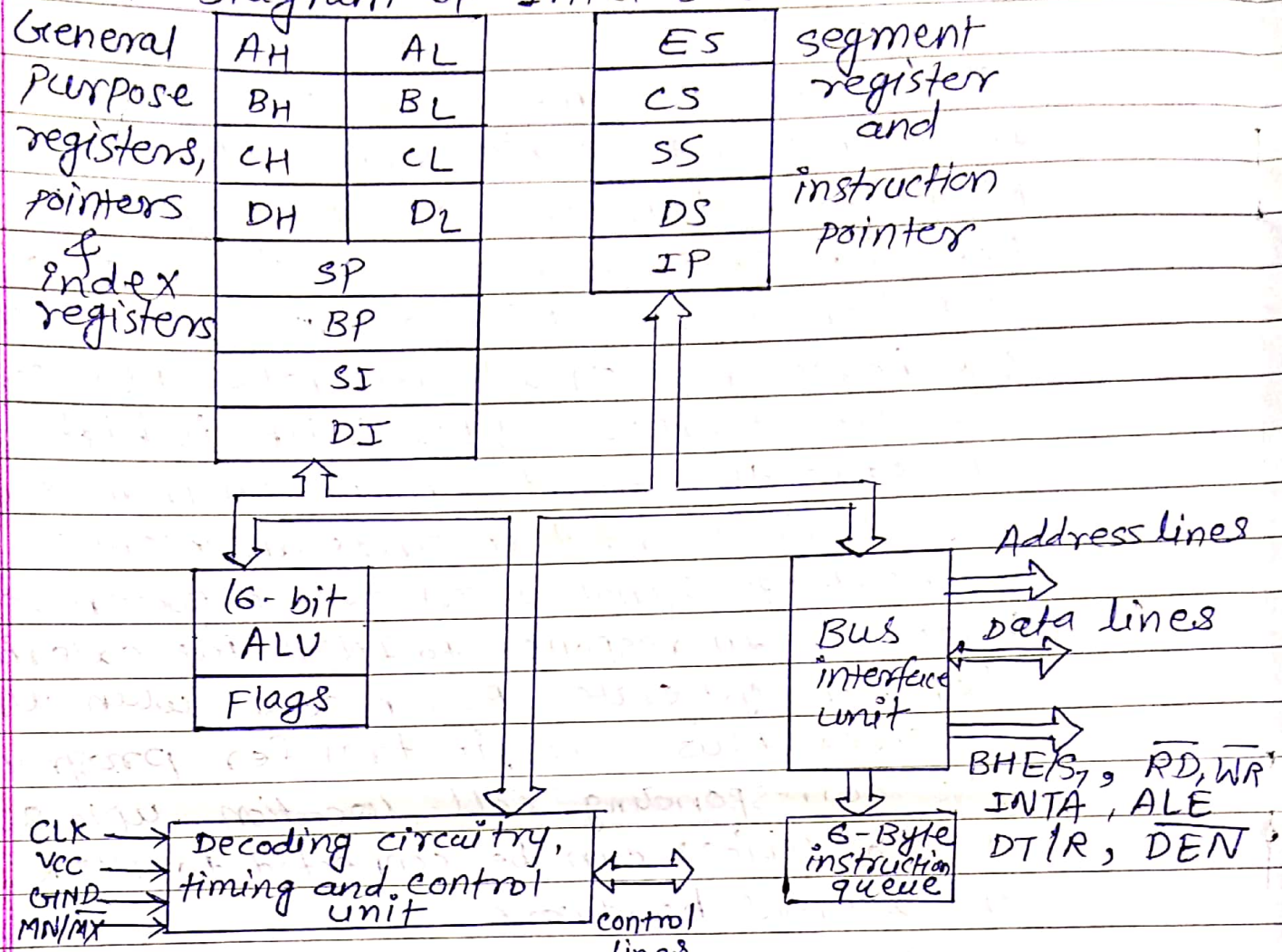
# Unit - IV

## Block Diagram of Intel 8086 microprocessor:




Block diagram of Intel 8086 UP

The 8086 contains two independent functional units: a bus interface unit (BIU) and an execution unit (EU). Fig. shows the block diagram of 8086 up. The general purpose registers, stack pointer, base pointer and index registers, ALU flag register (flags), instruction decoder and timing and control unit constitute execution unit (EU).

The segment registers, instruction pointer and 6-byte instruction queue are associated with the bus interface unit (BIU)

The BIU handles transfer of data and address between the processor and memory/IO

devices. It computes and sends out addresses, fetches instruction codes, stores fetched instruction codes in a first-in-first out register set called a queue, reads data from memory and I/O devices, writes data to memory and I/O devices. It relocates addresses of operands since it gets unrelocated operands addresses from EU. The execution unit tells BIU from where to fetch instruction or to read data.

The EU receives opecode of an instruction from the queue, decodes it and then executes it. While EU is decoding an instruction or executing an instruction, the BIU fetches instruction codes from the memory and stores them in the queue. The BIU and EU operate in parallel independently. This makes processing faster except in the cases of jump and call instructions, where the queue must be dumped and then reloaded from a new address.

While EU executes instructions, the BIU Fetches instructions. This type of overlapped operation of the functional units of a microprocessor is called pipelining. This technique has been extended to more than two functional unit in case of 32-bit and 64-bit microprocessor.

Registers of Intel 8086 –

The Intel 8086 contains the following registers:

i) General purpose registers
ii) Pointer and Index registers

iii) segment registers
iv) Instruction pointer
v) Status flags.

following fig. shows the register organization of Intel 8086 microprocessor

| | | | |
|---|---|---|---|
| Accumulator | AH | AL | General purpose Registers |
| Base | BH | BL | |
| Counter | CH | CL | |
| Data | DH | DL | |
| Stack pointer | SP | | pointer and Index Registers |
| Base pointer | BP | | |
| Source Index | SI | | |
| Destination Index | DI | | |
| code segment | CS | | segment Registers |
| Data segment | DS | | |
| Strack segment | SS | | |
| Extra segment | ES | | |
| Instruction pointer | IP | | |
| status registers | Flags | | |

- General purpose Registers:

There are four 16-bit general purpose registers: AX, BX, CX and DX. Each of these 16-bit registers are further subdivided into two 8-bit registers as shown below

| 16-Bit registers | 8-bit High-order Registers | 8-Bit Low-order Registers |
|---|---|---|
| AX | AH | AL |
| BX | BH | BL |
| CX | CH | CL |
| DX | DH | DL |

Register AX serves as an accumulator. Registers BX, CX and DX are used as general purpose registers. In addition to serving as general purpose registers they also serve as special purpose registers. As a special purpose register BX serve as a base register for the computation of memory address. In 8086 memory addresses are to be calculated using the contents of the segment register and effective memory address. This will be explained later on. Register CX is also used as a counter in case of multi-iteration instructions. When the content of CX becomes zero such instructions terminate the execution. DX register is also used for memory addressing when data are transferred between I/O port and memory using certain I/O instructions.

- Pointer and Index Registers:-
The following four registers are in the group of pointer and Index Registers

1. Stack pointer, SP
2. Base pointer, BP
3. Source Index, SI
4. Destination Index, DI

The function of SP is same as the function of stack pointer in Intel 8085. BP, SI and DI are used in memory address computation.

- Segment Register:-
There are four segment registers in 8086 as given below:

1. code segment Register, CS
2. Data segment Register, DS
3. stack segment Register, SS
4. Extra segment Register, ES

In an 8086 microprocessor-based system memory is divided into these four segments.

The code segment of the memory holds instruction codes of a program. The data, variables and constants given in the program are held in the data segment of the memory. stack segment holds addresses and data of subroutines. It also holds the contents of registers or memory locations given in PUSH instruction. Before attending an interrupt, the microprocessor saves the content of Program counter on the stack. Also, when CALL instruction is executed, before the execution of the subroutine, the address of the next instruction of the program is saved on the stack. The extra segment holds the destination addresses of some data of certain string instructions.

A segment register points to the starting address of a memory segment currently being used. for example, the code segment register points to the starting address of the code segment, the data segment register points to the starting address of the data segment. The maximum capacity of a segment may be upto 64-kbytes.

The 8086 instructions specify 16-bit memory address. The actual addresses are

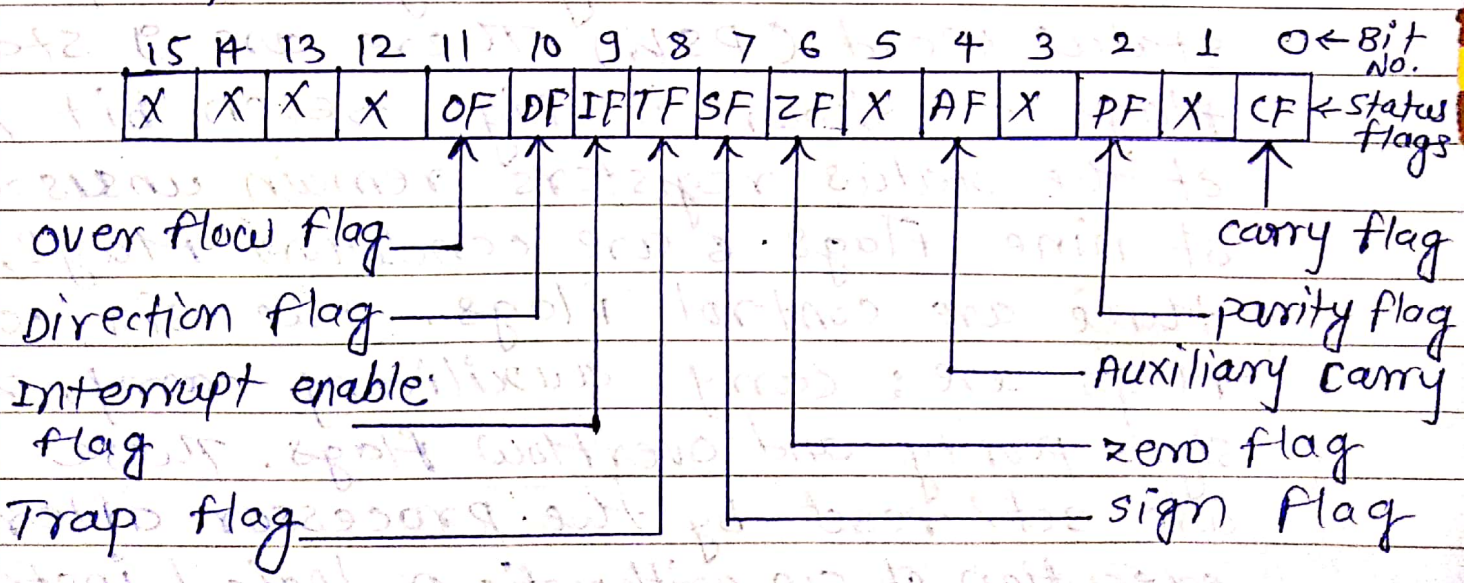
of 20 bits. They are calculated using the contents of the segment registers and effective memory address.

- Instruction pointer (IP): The instruction pointer in the 8086 µP acts as a program counter. It points to the address of the next instruction to be executed. Its contents is automatically incremented when the execution of a program proceeds further. The content ~~is auto~~ of the instruction pointer (IP) and the content of the code segment register are used to compute the memory address of the instruction code to be fetched. This is done during instruction fetch operation.

- Status Register :-

The 8086 contains a 16-bit status register. It is also called flag register or program status word (PSW). There are 9 status flags as shown in fig. seven bit position of the status registers remain unused. out of nine flags 6 are condition flags, and three are control flags. The six condition flags are: carry, auxiliary carry, zero, sign, parity and overflow flags. These flags are set/reset by the processor after the execution of an arithmetic or logical instruction. The three control flags are: trap (or trace) interrupt and directional flag. These flags are set/reset by the programmer as required

by certain instructions in the program.
The overflow flag is set to 1, if the result of a signed operation becomes out of range, otherwise it is reset i.e. it is made 0.
When the trap flag (TF) is set to 1, a program can be run in single-step mode.
The interrupt flag (IF) is set to 1 to enable INTR of 8086. If it is 0, INTR is disabled.
The directional flag (DF) is used in string operation. It can be set by STD instruction and cleared by CLD instruction. If it is set to 1, string bytes are accessed from higher memory addresses to lower memory address. When it is set to zero, the string bytes are accessed from lower memory addresses to higher memory addresses.




Status flags of Intel 8086

## 11.2 INTEL 8086

The 8086 is a 16-bit, N-channel, HMOS microprocessor. The term HMOS is used for "high-speed MOS". Its CMOS (Complementry MOS) version, the 80C86 is also available. It consumes less power. The 8086 draws 360 mA on 5 V whereas the 80C86 draws only 10 mA. The 8086 is manufactured for standard temperature range 32°F to 180°F as well as extended temperature range (40°F to +225°F). Its clock frequencies for its different versions are: 5, 8 and 10 MHz. It was introduced in 1978. It contains an electronic circuitry of 29000 transistors. It is built on a single semiconductor chip and packaged in a 40-pin IC package. The type of the package is DIP (Dual In-Line Package).

The 8086 uses 20 address lines and 16 data lines. It can directly address up to $2^{20}$ = 1 Mbytes of memory. The 16-bit data word is divided into a low-order byte and a high-order byte. The 20 address lines are time multiplexed lines. The 16 low-order address lines are time multiplexed with data, and the 4 high- order address lines are time multiplexed with status signals. Fig. 11.1 shows the pin diagram of Intel 8086.

AD0-AD15 are 16 low-order address lines. 8 LSBs of data are transmitted on AD0-AD7 and 8 MSBs of data on AD8-AD15. $\overline{BHE}$ at pin number 34 is multiplexed with status signals S7. The Intel 8284 clock generator/driver is used to generate the clock signal required for 8086 microprocessor. In

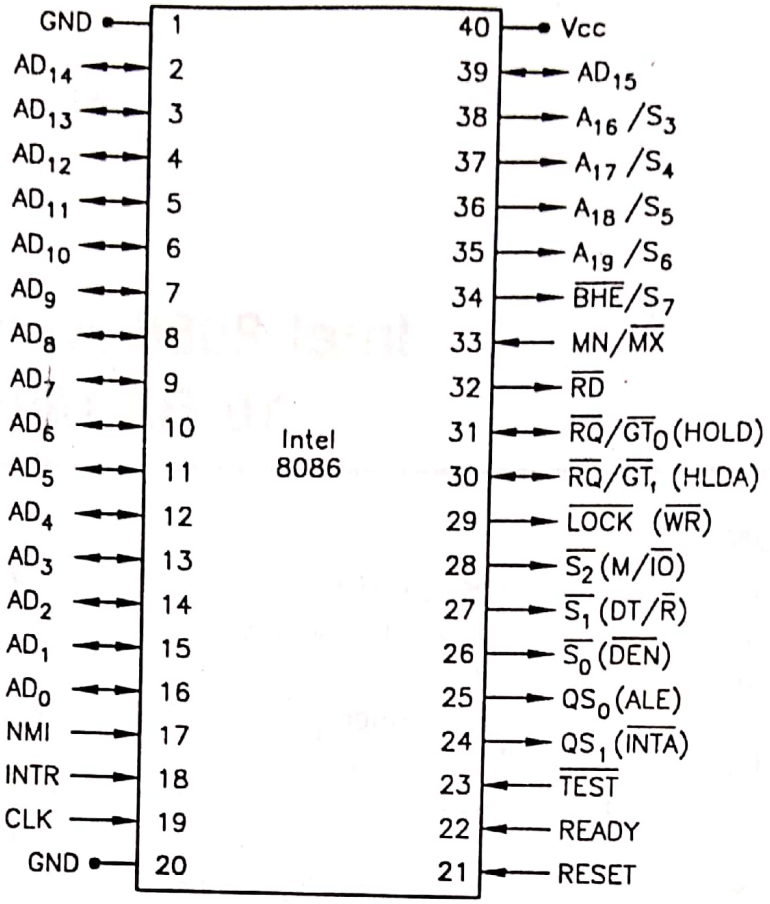



**Fig. 11.1** Pin Diagram of Intel 8086 Microprocessor

a microprocessor-based system when bus controller is required the Intel 8288 is used with 8086 CPU. In a single bus configuration the 8288 may not be used.

### 11.2.1 Pin Description of 8086

The description of the pins of 8086 is as follows :

**AD0-AD15.** (Bidirectional) Address/Data lines. These are low-order address bus. They are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A0-A15. When data are transmitted over AD lines the symbol D is used in place of AD, for example D0-D7, D8-D15 or D0-D15.

**A16-A19 (Output).** High-order address lines. These are multiplexed with status signals.

**A16/S3, A17/S4.** A16 and A17 are multiplexed with segment identifier signals S3 and S4.

**A18/S5.** A18 is multiplexed with interrupt status S5.

**A19/S6.** A19 is multiplexed with status signal S6.

**$\overline{\text{BHE}}$/S7 (Output).** Bus High Enable/Status. During T1 it is low. It is used to enable data onto the most significant half of data bus, D8-D15. 8-bit device connected to upper half of the data bus use $\overline{\text{BHE}}$ signal. It is multiplexed with status signal S7. S7 signal is available during T3 and T4.

**$\overline{\text{RD}}$ (Read).** This signal is used for read operation. It is an output signal. It is active when LOW.

**READY(Input).** The addressed I/O or memory sends acknowledgment through this pin. When HIGH it indicates that the peripheral is ready to transfer data.

**RESET (Input).** System reset. The signal is active HIGH.

**CLK (Input).** Clock. 5, 8 or 10 MHz.

**INTR** (Interrupt request)

**NMI (Input).** Non-maskable interrupt request.

**$\overline{\text{TEST}}$ (Input).** Wait for test control. When it is low the microprocessor continues execution otherwise waits.

**VCC.** Power supply, + 5 V d.c.

**GND.** Ground.

### 11.2.2 Operating Modes of 8086

There are two modes of operation for Intel 8086, namely the minimum mode and the maximum mode. When only one 8086 CPU is to be used in a microcomputer system the 8086 is used in the minimum mode of operation. In this mode the CPU issues the control signals required by memory and I/O devices. In a multiprocessor system it operates in the maximum mode. In case of maximum mode of operation control signals are issued by Intel 8288 bus controller which is used with 8086 for this very purpose. The level of the pin MN/$\overline{\text{MX}}$ decides the operating mode of 8086. When MN/$\overline{\text{MX}}$ is high the CPU operates in the minimum mode. When it is low the CPU operates in the maximum mode. From pin 24 to 31 issue two different sets of signals. One set of signals is issued when the CPU operates in the minimum mode. The other set of signals is issued when the CPU operates in the maximum mode. Thus the pins from 24 to 31 have alternate functions.

### 11.2.3 Pin Description for Minimum Mode

For the minimum mode of operation the pin MN/$\overline{\text{MX}}$ is connected to 5 V d.c. supply, i.e. MN/$\overline{\text{MX}}$ = VCC. The description of the pins from 24 to 31 for the minimum mode is as follows :

**$\overline{\text{INTA}}$(Output).** Pin No. 24. Interrupt acknowledge. On receiving interrupt signal the processor issues an interrupt acknowledge signal. It is active LOW.

**ALE(Output).** Pin No. 25. Address latch enable. It goes HIGH during T1. The microprocessor sends this signal to latch the address into the Intel 8282/8283 latch.

**$\overline{\text{DEN}}$(Output).** Pin No. 26. Data enable. When Intel 8286/8287 octal bus transceiver is used this signal acts as an output enable signal. It is active LOW.

**DT / $\overline{\text{R}}$(Output).** Pin No. 27. Data Transmit/Receive. When Intel 8286/8287 octal bus transceiver is used this signal controls the direction of data flow through the transceiver. When it is HIGH data are sent out. When it is LOW data are received.

**M / $\overline{\text{IO}}$ (Output).** Pin No. 28. Memory or I/O access. When it is HIGH the CPU wants to access memory. When it is LOW the CPU wants to access I/O device.

**$\overline{\text{WR}}$ (Output).** Pin No. 29. Write. When it is LOW the CPU performs memory or I/O write operation.

**HLDA(Output).** Pin No. 30. HOLD acknowledge. It is issued by the processor when it receives HOLD signal. It is active HIGH signal. When HOLD request is removed HLDA goes LOW.

**HOLD(Input).** Pin No. 31. Hold. When another device in microcomputer system wants to use the address and data bus, it sends a HOLD request to CPU through this pin. It is an active HIGH signal.

### 11.2.4 Pin Description For Maximum Mode

For the maximum mode of operation the pin MN/$\overline{\text{MX}}$ is made LOW. It is grounded. The description of the pins from 24 to 31 is as follows :

**QS1, QS0 (Output).** Pin Nos. 24, 25. Instruction Queue Status. Logics are given below :

| QS1 | QS0 | |
|---|---|---|
| 0 | 0 | No operation |
| 0 | 1 | 1st byte of opecode from queue |
| 1 | 0 | Empty the queue |
| 1 | 1 | Subsequent byte from queue |

**$\overline{S0}$, $\overline{S1}$, $\overline{S2}$ (Output).** Pin Nos. 26, 27, 28. Status signals. These signals are connected to the bus controller Intel 8288. The bus controller generates memory and I/O access control signals. Table 11.1 shows the logic for status signals.

**Table 11.1 Logic for Status Signals**

| $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | |
|---|---|---|---|
| 0 | 0 | 0 | Interrupt acknowledge |
| 0 | 0 | 1 | Read data from I/O port |
| 0 | 1 | 0 | Write data into I/O port |
| 0 | 1 | 1 | Halt |
| 1 | 0 | 0 | Opcode fetch |
| 1 | 0 | 1 | Memory read |
| 1 | 1 | 0 | Memory write |
| 1 | 1 | 1 | Passive state. |

**$\overline{\text{LOCK}}$ (Output).** Pin No. 29. It is an active LOW signal. When it is LOW all interrupts are masked and no HOLD request is granted. In a multiprocessor system all other processors are informed by this signal that they should not ask the CPU for relinquishing the bus control.

**$\overline{RQ}/\overline{GT}_1$, $\overline{RQ}/\overline{GT}_0$.** (Bidirectional). Pin Nos. 30, 31. Local Bus Priority Control. Other processors ask the CPU through these lines to release the local bus. $\overline{RQ}/\overline{GT}_0$ has higher priority than $\overline{RQ}/\overline{GT}_1$.

In the maximum mode of operation signals $\overline{WR}$, ALE, $\overline{DEN}$, DT/$\overline{R}$ etc. are not available directly from the processor. These signals are available from the controller 8288.